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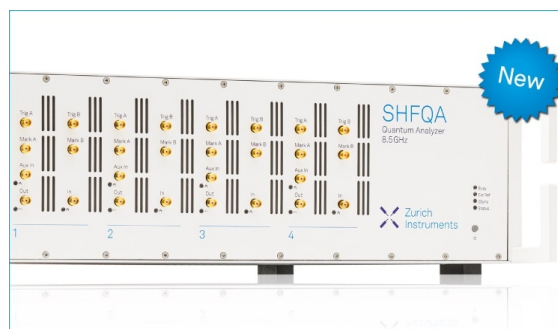
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ABSTRACT

This work presents a tri-gate GaN junction high-electron-mobility transistor (JHEMT) concept in which the p-n junction wraps around the AlGaIn/GaN fins in the gate region. This tri-gate JHEMT differs from all existing GaN FinFETs and tri-gate HEMTs, as they employ a Schottky or a metal-insulator-semiconductor (MIS) gate stack. A tri-gate GaN JHEMT is fabricated using p-type NiO with the gate metal forming an Ohmic contact to NiO. The device shows minimal hysteresis and a subthreshold slope of 63 ± 2 mV/decade with an on-off current ratio of 10^8 . Compared to the tri-gate MISHEMTs fabricated on the same wafer, the tri-gate JHEMTs exhibit higher threshold voltage (V_{TH}) and achieve positive V_{TH} without the need for additional AlGaIn recess. In addition, this tri-gate JHEMT with a fin width of 60 nm achieves a breakdown voltage (BV) > 1500 V (defined at the drain current of $1 \mu\text{A}/\text{mm}$ at zero gate bias) and maintains the high BV with the fin length scaled down to 200 nm. In comparison, the tri-gate MISHEMTs with narrower and longer fins show punch-through at high voltages. Moreover, when compared to planar enhancement mode HEMTs, tri-gate JHEMTs show significantly lower channel sheet resistance in the gate region. These results illustrate a stronger channel depletion and electrostatic control in the junction tri-gate compared to the MIS tri-gate and suggest great promise of the tri-gate GaN JHEMTs for both high-voltage power and low-voltage power/digital applications.

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The AlGaIn/GaN high electron mobility transistor (HEMT) is gaining increased adoption in RF and power applications, owing to the high critical field of GaN and the high electron mobility in two-dimensional electron gas (2DEG). Recently, low-voltage GaN HEMTs have also been used in power ICs for monolithic integration with power devices.¹ While all commercial HEMTs use 2D gate structures, the three-dimensional (3D) FinFET/tri-gate structure,² the enabling technology for Si CMOS scaling,³ has been recently implemented in GaN HEMTs for RF^{4–13} and power^{14–21} applications. The GaN FinFETs and tri-gate HEMTs enabled a superior on-off current ratio, subthreshold slope (SS), linearity, and transconductance (g_m). Vertical GaN FinFETs have also been demonstrated with high performance for kilovolt applications.^{22,23}

Despite these early demonstrations, tri-gate HEMTs still face several challenges in realizing enhancement-mode (E-mode) operation, which is highly desired for digital and power applications. Specifically,

E-mode in high-voltage transistors requires not only a positive threshold voltage (V_{TH}) but also the capability to block high drain voltage at zero gate bias (V_G).²⁴ The high 2DEG density typically necessitates a fin width below 30 nm for full 2DEG depletion,²⁵ and it often induces drain-induced-barrier-lowering (DIBL).²⁶ Recently, an E-mode tri-gate HEMT with a fin width down to 20 nm and a large work function (WF) gate demonstrated a high breakdown voltage (BV) over 1 kV.¹⁸ To relax the need for aggressive fin scaling, an additional AlGaIn recess^{14,19} or charge trap dielectrics²⁰ have been utilized to assist the 2DEG depletion in the tri-gate device. However, these structures require additional etching or unconventional multi-layer dielectrics.

In this Letter, we propose a significantly distinct tri-gate device concept, the tri-gate junction HEMT (JHEMT). While all existing GaN FinFETs and tri-gate HEMTs employ a Schottky or a metal-insulator-semiconductor (MIS) gate stack, the tri-gate JHEMT relies on the p-n junction wrapping around the AlGaIn/GaN fins [Fig. 1(a)].

The p-n junction can offer stronger depletion than the MIS structure owing to a larger built-in potential (V_{bi}) and the obviation of voltage drop in the insulating dielectrics,²² thereby making it easier to realize the E-mode operation, suppress the DIBL, and prevent the punch-through. It also eliminates the MIS inversion charges at the fin sidewalls and trench bottoms, thereby reducing the gate charge and the parasitic conduction along the sidewall channels.²⁷ Compared to the planar p-gate HEMT, such as the gate injection transistor (GIT),²⁸ the tri-gate JHEMT offers stronger depletion and gate control over channel electrostatics.

While p-GaN is a natural p-type material for the proposed tri-gate JHEMT, sub-micron selective-area p-type doping is still not viable in GaN. As an alternative, in this work, we demonstrate a GaN tri-gate JHEMT using NiO, a p-type oxide that possesses a high hole concentration and can form high-quality hetero-junctions on AlGaN^{29–31} and GaN^{32,33} with a relatively large V_{bi} (1–1.5 eV). In addition, NiO can be sputtered at room temperature, which simplifies the junction tri-gate fabrication. Our fabricated E-mode tri-gate JHEMTs exhibit a higher V_{TH} , lower hysteresis, and lower SS compared to the tri-gate MISHEMTs fabricated on the same wafer, as well as a BV over 2000 V at zero V_G . Their performance is also benchmarked with the tri-gate MISHEMTs and planar E-mode devices, followed by an in-depth discussion on their application spaces.

The epitaxial structure consists of 10 nm *in situ* SiN_x, 3 nm GaN, 22 nm Al_{0.25}Ga_{0.75}N, 420 nm i-GaN, and a buffer layer, all grown on a 6-inch Si substrate by metal-organic chemical vapor deposition. The 2DEG density and sheet resistance are $8.5 \times 10^{12} \text{ cm}^{-2}$ and $480 \Omega/\text{sq}$, respectively. As shown in Fig. 1(a), the tri-gate GaN MISHEMTs and JHEMTs are fabricated on the same wafer with the fin width (W_{Fin}) ranging from 40 nm to 120 nm. A relatively large fin spacing (S_{Fin}) of 150 nm is chosen to allow the fabrication of tri-gate JHEMTs with different NiO thicknesses, which is critical toward understanding the physics of tri-gate JHEMTs. The fin length (L_{Fin}) varies from 200 nm

to 1 μm and the gate length (L_G) is fixed at 2 μm . The gate-to-source distance (L_{GS}) is 2 μm , and the gate-to-drain distance (L_{GD}) varies from 6 μm to 21 μm .

The device fabrication starts with SiN removal and the deposition of 40 nm SiO₂ via plasma-enhanced chemical vapor deposition (PECVD), followed by electron-beam lithography to lift off Cr as the hard mask for subsequent fin etch. The 140-nm-high fins are etched by reactive ion etching and then rinsed with 5% tetramethylammonium hydroxide (TMAH) to remove etch damage.³⁴ PECVD SiO₂ protects the top fin surface in the TMAH treatment. Ti/Al/Ni/Au Ohmic contacts are then formed for the source and drain.

A self-aligned process³⁵ is used to lift off the NiO and gate metal in the same lithography step. NiO is deposited in a magnetron sputtering system using a NiO target in an Ar (70%)/O₂ (30%) atmosphere at 25 °C. The chamber pressure is 3 mTorr, and the RF power is 100 W. Figure 1(b) shows the scanning electron microscopy (SEM) images of the GaN fins before and after NiO sputtering, verifying the conformal NiO coverage. Three samples with planar NiO thicknesses of 50 nm, 100 nm, and 150 nm are fabricated. The sidewall sputtering rate is found to be $\sim 1/3$ of the planar rate. In the 50-nm and 100-nm samples, NiO fills the inter-fin trenches to the levels below the 2DEG; in the 150 nm sample, NiO fully fills the trenches. A Ni/Au stack is used for the gate, which forms an Ohmic contact to NiO. Figure 1(c) shows the Hall measurements for the Ni pads on NiO using the van der Pauw method. The linear I-V curve verifies the good Ohmic contact between Ni and NiO. A hole concentration and mobility of $5 \times 10^{19} \text{ cm}^{-3}$ and $0.7 \text{ cm}^2/\text{V s}$ are extracted for the sputtered p-NiO, respectively. For the tri-gate MISHEMTs, 15 nm Al₂O₃ is deposited by atomic layer deposition at 275 °C as the gate dielectric and the same Ni/Au is used for the gate metal. Finally, PECVD SiN_x is deposited for the passivation of both tri-gate JHEMTs and tri-gate MISHEMTs.

Although the V_{bi} values between p-NiO and AlGaN³¹ or GaN³² have been reported previously, there have been no studies on V_{bi} between p-NiO and the 2DEG, which is critical for understanding the sidewall electrostatics in our junction tri-gate structure. Figure 2(a) shows the simulated band diagram of the NiO/GaN/AlGaN/GaN stack using the material properties of sputtered NiO,³² which predicts a V_{bi} value of 1.2–1.3 eV between 2DEG and p-NiO. To measure the V_{bi} value experimentally, a NiO/2DEG p-n junction diode is fabricated, where the sputtered p-NiO forms contact with 2DEG at a mesa sidewall [see Fig. 2(b)]. Figure 2(c) shows the I-V characteristics of this NiO/2DEG diode. The current starts to increase at ~ 1.3 V, which verifies the simulated V_{bi} .

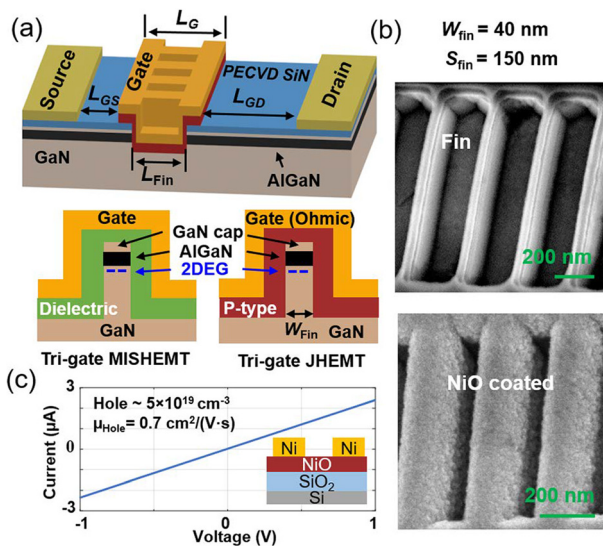


FIG. 1. (a) Schematic of the tri-gate GaN MISHEMT and tri-gate GaN JHEMT. (b) SEM image of the fins before and after the NiO sputtering. (c) I-V curve between two Hall Ni pads on p-NiO, showing a good Ohmic contact.

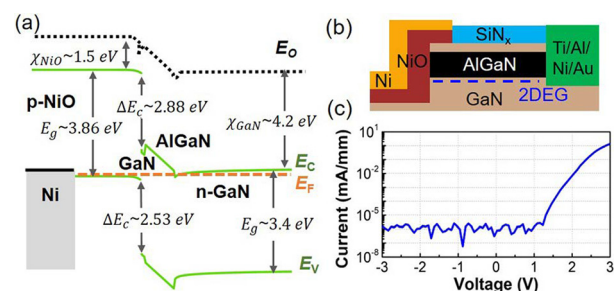


FIG. 2. (a) Band diagram of the NiO/GaN/AlGaN/GaN structure. (b) Schematic and (c) I-V characteristics of the fabricated NiO/2DEG junction diode.

Figure 3(a) shows the transfer characteristics ($V_{DS} = 0.25$ V, linear region) of the tri-gate JHEMTs with planar NiO thicknesses of 50 nm, 100 nm, and 150 nm. The current density of all transistors in this work is normalized by the total gate width (50 μm). Due to a smaller sidewall sputtering rate, the 50-nm-NiO tri-gate JHEMT has thin (<16 nm) and even incomplete sidewall coverage, leading to higher leakage current and higher SS. When NiO is thicker, thus ensuring complete sidewall coverage, the junction depletion occurs in GaN due to the high hole concentration in NiO, resulting in a V_{TH} value that is independent of the NiO thickness. This is validated by the almost identical transfer characteristics of the tri-gate JHEMTs with 100 nm and 150 nm NiO [see Fig. 3(a)]. Note that this behavior is different from the tri-gate MISHEMT, wherein V_{TH} strongly depends on the thickness (and capacitance) of the insulating dielectrics. This difference reflects the inherent benefits of the junction gate in eliminating the voltage drop in the gate dielectric. The tri-gate JHEMTs with 100 nm and 150 nm NiO show a minimum SS of 63 ± 2 mV/decade with an on-off current ratio of $\sim 10^8$. For clarity, the devices discussed through the remainder of this work all have a NiO thickness of 100 nm.

Figure 3(b) shows the double-sweep transfer characteristics ($V_{DS} = 5$ V, saturation region) of the tri-gate JHEMTs and MISHEMTs with 60 nm W_{Fin} . The tri-gate JHEMT has a V_{TH} value of

0.45 V [extracted at the drain current (I_D) of $1 \mu\text{A}/\text{mm}$] and a hysteresis below 0.1 V, while the tri-gate MISHEMTs show a negative V_{TH} and ~ 0.6 V hysteresis. The close-to-60 mV/decade SS and small hysteresis in tri-gate JHEMTs suggest a very small interface state (D_{it}) in the NiO-based junction gate, whereas the larger SS (minimum 70 ± 5 mV/decade) and hysteresis in the tri-gate MISHEMTs suggest a higher $\text{Al}_2\text{O}_3/\text{GaN}$ D_{it} .^{14,36} The gate leakage current (I_G) in tri-gate JHEMTs is very low at $V_G < 1$ V and starts to increase when V_G exceeds the V_{bi} value between NiO and 2DEG. Hence, a similar gate driver to the one used for GaN GITs³⁷ is preferred for the tri-gate JHEMTs, and the practical on-state V_G is 3–4 V for the NiO-based tri-gate JHEMTs. In future tri-gate JHEMT devices, the V_G margin can be further increased by using the heterogeneous or homogenous p-n junctions with higher V_{bi} than that of the p-NiO/2DEG junction. For example, the homogeneous p-GaN/2DEG junction³⁸ has been recently demonstrated with a high V_{bi} (~ 3 V) and an excellent on-off current ratio, which could be a good candidate for future junction tri-gates.

Figure 3(c) shows the W_{Fin} -dependent transfer characteristics of the tri-gate MISHEMTs and JHEMTs, where V_{TH} increases with a decreased W_{Fin} in both types of devices. Tri-gate JHEMTs show a 1–1.5 V higher V_{TH} than the tri-gate MISHEMTs with the same W_{Fin} , validating the stronger 2DEG depletion in the junction tri-gate. The tri-gate MISHEMT starts to see a positive V_{TH} at 40 nm W_{Fin} , while the tri-gate JHEMT does at 60 nm W_{Fin} . The 40 nm tri-gate JHEMT shows a V_{TH} value of 1.1 V. V_{TH} in future tri-gate JHEMTs can be further increased by either using the p-n junctions with higher V_{bi} or the barrier structures allowing more pronounced strain relaxation in narrow fins (e.g., AlN/GaN barrier). Figure 3(d) shows the output characteristics of the 60-nm tri-gate JHEMTs and 40-nm tri-gate MISHEMTs with a similar V_{TH} value. The higher current density in the tri-gate JHEMT is mainly due to the larger gate area available for current conduction, i.e., filling factor (FF) = $W_{Fin}/(W_{Fin} + S_{Fin})$. The FF is 0.28 for 60-nm tri-gate JHEMTs and 0.21 for 40-nm tri-gate MISHEMTs. The E-mode 60-nm tri-gate JHEMT shows an on resistance (R_{on}) of 9.42 $\Omega\text{-mm}$.

Figure 3(e) shows the box charts of the W_{Fin} -dependent V_{TH} of the tri-gate MISHEMTs and JHEMTs, revealing a relatively good V_{TH} homogeneity with a variation of ± 0.04 V $\sim \pm 0.07$ V in JHEMTs and ± 0.08 V $\sim \pm 0.2$ V in MISHEMTs. The smaller V_{TH} variation in tri-gate JHEMTs is attributable to the smaller D_{it} in the junction tri-gate. Figure 3(f) shows temperature-dependent transfer characteristics of the tri-gate JHEMTs up to 150 $^\circ\text{C}$, revealing a good thermal stability in V_{TH} (0.45 V at 25 $^\circ\text{C}$ –0.28 V at 150 $^\circ\text{C}$) and off-state I_D and I_G . This suggests the good thermal stability of the physical properties of the sputtered p-NiO.

The leakage and BV in high-voltage FinFETs are usually determined by both the E-field management and the potential barrier in the fin (Ψ_{Fin}).²⁴ When Ψ_{Fin} is high, the drain leakage current is low and the BV is E-field limited; otherwise, punch-through will occur due to DIBL. Ψ_{Fin} in a fin gate generally decreases with increased W_{Fin} , reduced L_{Fin} , and more positive V_G .²⁴ Figure 4(a) shows the off-state I-V characteristics of the 60-nm tri-gate JHEMT with various L_{GD} values. The I_D value is $\sim 10^{-7}$ A/mm and BV scales with L_{GD} at zero V_G , suggesting a high Ψ_{Fin} up to >2000 V V_D . Figure 4(b) shows the off-state I-V characteristics of the 40-nm tri-gate MISHEMTs at V_G values of 0 V and -2 V. At a V_G value of -2 V, their leakage and BV

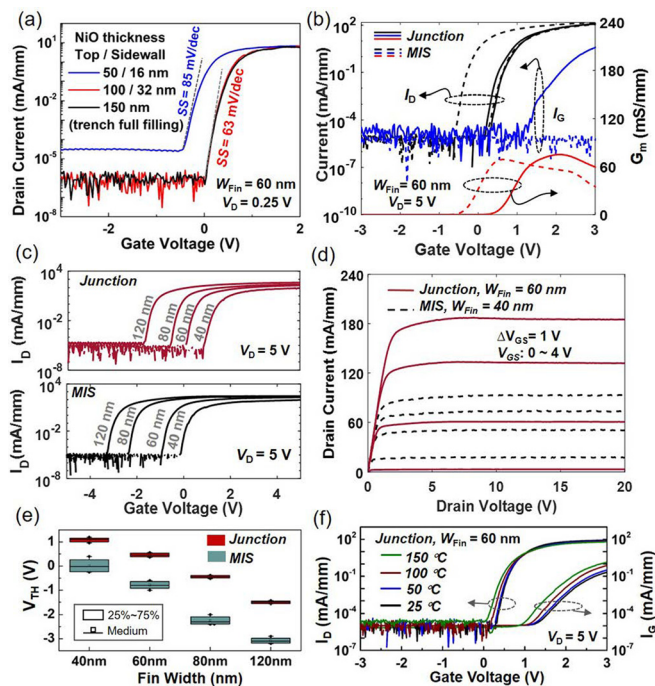


FIG. 3. Transfer characteristics of (a) tri-gate JHEMTs with various NiO thicknesses, (b) tri-gate JHEMTs (solid lines) and tri-gate MISHEMTs (dashed lines) with 60 nm W_{Fin} (I_D in black, I_G in blue, and g_m in red), and (c) the two types of tri-gate devices with different W_{Fin} values. (d) Output characteristics of 60-nm tri-gate JHEMTs (solid lines) and 40-nm tri-gate MISHEMTs (dashed lines). (e) Box charts of the W_{Fin} -dependent V_{TH} of the tri-gate JHEMTs and MISHEMTs. 7 devices in different dies are measured for each type of device. (f) Temperature-dependent transfer characteristics of the tri-gate JHEMTs at 25–150 $^\circ\text{C}$. All devices in this figure have an L_{Fin} value of 500 nm and an L_{GD} value of 6 μm .

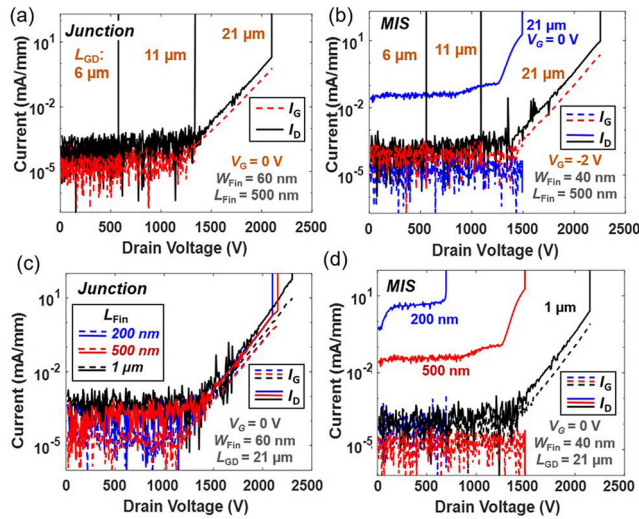


FIG. 4. Off-state I-V characteristics of (a) 60-nm tri-gate JHEMTs with various L_{GD} values at 0 V V_G , (b) 40-nm tri-gate MISHEMTs with various L_{GD} values at 0 V V_G (I_D in blue solid lines and I_G in blue dashed lines) and -2 V V_G (I_D in black solid lines and I_G in red dashed lines), as well as (c) 60-nm tri-gate JHEMTs and (d) 40-nm tri-gate MISHEMTs with various L_{Fin} values at 0 V V_G (I_D in solid lines and I_G in dashed lines).

are similar to those of the 60-nm tri-gate JHEMTs. However, at zero V_G , the leakage current increases by at least 10^3 -fold and the BV is significantly compromised, due to punch-through. This suggests an intrinsically lower Ψ_{Fin} in the MIS tri-gate as compared to the junction tri-gate.

Figures 4(c) and 4(d) show the off-state I-V characteristics of the 60-nm tri-gate JHEMTs and 40-nm tri-gate MISHEMTs with various L_{Fin} values at zero V_G . The 60-nm tri-gate JHEMT maintains low leakage current and >2000 V BV when L_{Fin} is reduced to 200 nm. In contrast, the tri-gate 40-nm MISHEMT shows punch-through at 200 nm and 500 nm L_{Fin} and can only realize the high BV with 1 μm L_{Fin} . These results suggest the gate scaling capability of tri-gate JHEMTs, which would bring performance advancement in all power, RF, and digital HEMTs (e.g., smaller R_{on} and capacitance and higher cutoff frequency). Note that all the above off-state I-V characteristics are measured with the Si substrate floating to compare the inherent fin-gate limitations on the device BV . The substrate-grounded BV values of both the non-punch-through tri-gate MISHEMTs and JHEMTs are ~ 1200 V, limited by the vertical buffer leakage and breakdown in the GaN-on-Si wafer.

To further understand the leakage current in tri-gate HEMTs, physics-based 3D device TCAD simulation is performed in Silvaco Atlas, based on similar models previously developed for GaN FinFETs.²⁴ The 2DEG density in miniaturized fins is determined via calibration using experimental I-V characteristics. As illustrated in Fig. 5(a), the simulated conduction band energy is extracted at a side-view fin cross section and a top-view cross section on the 2DEG plane, for 40-nm tri-gate MISHEMTs [see Fig. 5(b)] and 60-nm tri-gate JHEMTs [see Fig. 5(c)] with 500 nm L_{Fin} , at both 0 V V_G and 1000 V V_{DS} . The lowest Ψ_{Fin} in the tri-gate fin channel is found to be at the 2DEG in the middle of the fin. Ψ_{Fin} is below 0.1 eV in the 40-nm

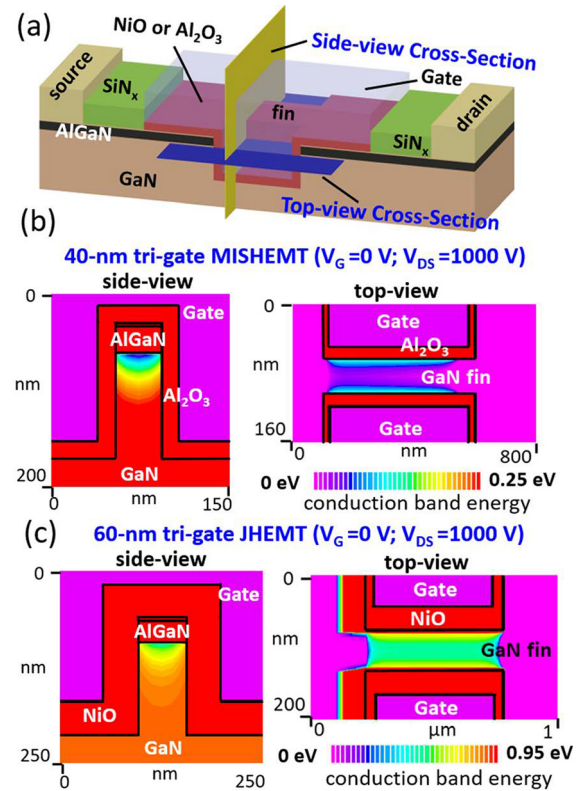


FIG. 5. (a) Illustration of the positions of the side-view and top-view cross sections. Simulated distribution of conduction band energy at the two cross sections in (b) 40-nm tri-gate MISHEMTs and (c) 60-nm tri-gate JHEMTs with 500 nm L_{Fin} at a V_G value of 0 V and a V_{DS} value of 1000 V.

tri-gate MISHEMTs, but above 0.55 eV in the 60-nm tri-gate JHEMTs. This explains the higher leakage current and punch-through observed in the 40-nm tri-gate MISHEMTs at zero V_G .

Table I compares the key device metrics of our E-mode tri-gate JHEMTs and the state-of-the-art E-mode tri-gate GaN MISHEMTs, as well as the planar E-mode HEMTs based on p-GaN gate³⁹ and AlGaN recess.⁴⁰ In all tri-gate GaN HEMTs, our tri-gate JHEMTs show the lowest SS and one of the highest BV , as well as realize the E-mode with a relatively large W_{Fin} and without the need for additional barrier recess. They also show one of the lowest R_{on} values in all tri-gate HEMTs with a similar FF (~ 0.3). To further compare different gate stacks, the device R_{on} components are separated,²⁰

$$R_{on} = 2R_C + R_A + R_G = 2R_C + R_{2DEG-SH}(L_{SG} + L_{GD}) + \overline{R_{G-SH}}L_G \\ = 2R_C + R_{2DEG-SH}(L_{SG} + L_{GD}) + \frac{KC_G}{\mu_G} \frac{1}{V_G - V_{TH}} L_G, \quad (1)$$

where R_C , R_A , R_G , and $R_{2DEG-SH}$ are the contact resistance, access-region channel resistance, gate-region channel resistance, and 2DEG sheet resistance, respectively. $\overline{R_{G-SH}}$ is the averaged channel sheet resistance in the gate region, which is dependent on C_G , the gate-to-2DEG unit capacitance, μ_G , the electron mobility, and $V_G - V_{TH}$, the gate overdrive. $2R_C + R_A$ can be extracted either by using the reported R_C and $R_{2DEG-SH}$ or from the intercept in the $R_{on}(V_G) \sim 1/(V_G - V_{TH})$

TABLE I. Comparison of device technologies and key metrics of various E-mode AlGaIn/GaN HEMTs.

References	Device technologies	W_{Fin} (nm)	L_{Fin} (μm)	V_{TH}^{a} (V)	SS (mV/dec.)	BV^{b} (V) at 1 $\mu\text{A}/\text{mm}$	Destructive BV^{b} (V)	R_{on}^{d} ($\Omega\text{-mm}$)	R_{G}^{d} ($\Omega\text{-mm}$)	$\overline{R_{\text{G-SH}}}$ d (k Ω/sq)	FF
This work	Junction tri-gate	60 (40)	0.2–0.5	0.45 (1.1)	63 ± 2	600–1500	600–2200	9.4–17	2.7	1.35	0.28
	MIS tri-gate	40	1	0.1	70 ± 5	600–1500	600–2100	11.4–19	4.7	2.35	0.21
18	MIS tri-gate + high WF gate metal	20	0.7	0.6	110	1080 ^c	N/A	10	~5.6	~2.2	0.3
14	MIS tri-gate + AlGaIn recess	120	0.66	0.53	86 ± 9	562	562	15.4	~7.2	~3.6	0.29
19	MIS tri-gate + AlGaIn recess	200	0.7	1.4	95 ± 3	1700	2100	8	~2.8	~1.4	0.66
20	MIS tri-gate + trap charge gate oxide	100	0.6	2.6	73	788	~1000	5	~1.2	~0.8	0.48
39	planar p-GaN gate	N/A	N/A	1.3	90	650 ^c	~700	13.5	~9	~11.2	1
40	planar AlGaIn recess	N/A	N/A	1.6	N/A	~600	~600	22.7	~13.2	~8.8	1

^aExtracted at a drain current of 1 $\mu\text{A}/\text{mm}$.

^bAll BV extracted at zero V_{G} .

^c BV measured with the substrate grounded; all other BV values in the table are measured with the substrate floating.

^dAll R_{on} , R_{G} , and $R_{\text{G-SH}}$ extracted at $V_{\text{G}} - V_{\text{TH}} \approx 4\text{V}$.

fitting with the $R_{\text{on}}(V_{\text{G}})$ extracted from the reported output characteristics. Subsequently, R_{G} and $\overline{R_{\text{G-SH}}}$ are extracted at a 4 V gate overdrive.

As shown in Table I, all tri-gate devices show significantly lower $\overline{R_{\text{G-SH}}}$ than planar p-gate HEMTs or recess HEMTs, as the tri-gate preserves the 2DEG channel in the gate region with superior gate control. In comparison, the planar p-gate HEMT typically has a thick p-GaN that separates the gate far away from 2DEG, leading to a small C_{G} ; the recessed gate replaces the 2DEG channel with a MIS channel under the gate, which significantly degrades μ_{G} . In tri-gate HEMTs, $\overline{R_{\text{G-SH}}}$ can be further lowered with an increased FF. Compared to the tri-gate MISHEMTs with a similar FF, our tri-gate JHEMT shows a lower $\overline{R_{\text{G-SH}}}$. It also shows the smallest L_{Fin} in all high-voltage tri-gate HEMTs. The lower $\overline{R_{\text{G-SH}}}$ and L_{Fin} suggest significant advantages in R_{G} reduction. Thus, the tri-gate JHEMT is promising for not only high-voltage power switches but also the low-voltage applications where the HEMT R_{on} would be increasingly contributed by R_{G} (as $\overline{R_{\text{G-SH}}}$ is much larger than $R_{\text{2DEG-SH}}$). The low SS in our tri-gate JHEMTs further strengthens their potential for low-voltage applications.

In summary, we propose the tri-gate GaN JHEMT concept, which differs from all existing tri-gate GaN MISHEMTs, and demonstrate it using a p-type NiO and Ohmic gate contact. The tri-gate GaN JHEMTs show a near-60 mV/decade SS and minimal hysteresis, suggesting low D_{it} . They exhibit higher V_{TH} than tri-gate GaN MISHEMTs, achieve the E-mode operation without additional gate recess, and demonstrate over 2 kV BV at zero V_{G} and scaled L_{Fin} , which all illustrate the stronger electrostatic control in the junction tri-gate compared to the MIS tri-gate. When compared to planar E-mode GaN HEMTs, they also show a significantly lower channel sheet resistance in the gate region. These results show the great potential of tri-gate GaN JHEMTs for both high-voltage power and low-voltage power/digital applications.

AUTHORS' CONTRIBUTIONS

Y.M. and M.X. contributed equally to this work.

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DATA AVAILABILITY

The data that support the findings of this study are available within this article.

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