Barrier-Engineered Arsenide–Antimonide Heterojunction Tunnel FETs With Enhanced Drive Current

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***Abstract*—In this letter, we experimentally demonstrate enhancement in drive current $I_{\rm ON}$ and reduction in drain-induced barrier thinning (DIBT) in arsenide–antimonide staggered-gap heterojunction (hetj) tunnel field-effect transistors (TFETs) by engineering the effective tunneling barrier height $\rm Eb_{eff}$ from 0.58 to 0.25 eV. Moderate-stagger $\rm GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ ($\rm Eb_{eff} = 0.31$ eV) and high-stagger $\rm GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ ($\rm Eb_{eff} = 0.25$ eV) hetj TFETs are fabricated, and their electrical results are compared with the $\rm In_{0.7}Ga_{0.3}As$ homojunction (homj) TFET ($\rm Eb_{eff} = 0.58$ eV). Due to the 57% reduction in $\rm Eb_{eff}$, the $\rm GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetj TFET achieves 253% enhancement in $I_{\rm ON}$ over the $\rm In_{0.7}Ga_{0.3}As$ homj TFET at $V_{DS} = 0.5$ V and $V_{GS} - V_{\rm OFF} = 1.5$ V. With electrical oxide thickness (Toxe) scaling from 2.3 to 2 nm, the enhancement further increases to 350%, resulting in a record high $I_{\rm ON}$ of 135 μA/μm and 65% reduction in DIBT at $V_{DS} = 0.5$ V.**

***Index Terms*—GaAsSb, InGaAs, stagger, tunnel field-effect transistors (TFETs).**

I. Introduction

INTERBAND tunnel field-effect transistors (TFETs) are being extensively explored as a low $V_{\rm CC}$ (0.5 V and below) logic switch owing to their ability to show sub-kT/q steep switching [1]–[4]. A point switching slope (SS) less than 60 mV/dec has been already demonstrated at room temperature [1], [2]. However, the drive current $I_{\rm ON}$ demonstrated to date are significantly lower than the metal–oxide–semiconductor field-effect transistors (MOSFETs) mainly due to the large source-side effective tunneling barrier height $\rm Eb_{eff}$ [1]–[3].

Mixed arsenide–antimonide-based lattice-matched heterojunctions ($\rm GaAs_xSb_{1-x}/In_yGa_{1-y}As$) provide a wide range of compositionally tunable $\rm Eb_{eff}$ [5]. With increasing Sb and In compositions, $\rm Eb_{eff}$ can be reduced from 0.5 eV ($x = 0.5,\ y = 0.53$) to 0 eV ($x = 0.1,\ y = 1$), and hence, the TFET $I_{\rm ON}$ can approach the MOSFET level without compromising the steep switching and high $I_{\rm ON}/I_{\rm OFF}$ property desirable in a low-power logic switch.

In this letter, we demonstrate n-channel moderate-stagger $\rm GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ ($\rm Eb_{eff} = 0.31$ eV) and high-stagger $\rm GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ ($\rm Eb_{eff} = 0.25$ eV) heterojunction (hetj) TFETs and compare their electrical results with the $\rm In_{0.7}Ga_{0.3}As$ homojunction (homj) TFET ($\rm Eb_{eff} = 0.58$ eV). By scaling $\rm Eb_{eff}$ from 0.58 to 0.25 eV, with the electrical oxide thickness (Toxe) being 2.3 nm, we demonstrate 253% enhancement in drive current at $V_{DS} = 0.5$ V and $V_{GS} - V_{\rm OFF} = 1.5$ V, $V_{\rm OFF}$ being the gate voltage corresponding to $I_{\rm OFF} = 5$ nA/μm. By further scaling Toxe to 2 nm, the enhancement in drive current is further shown to increase to

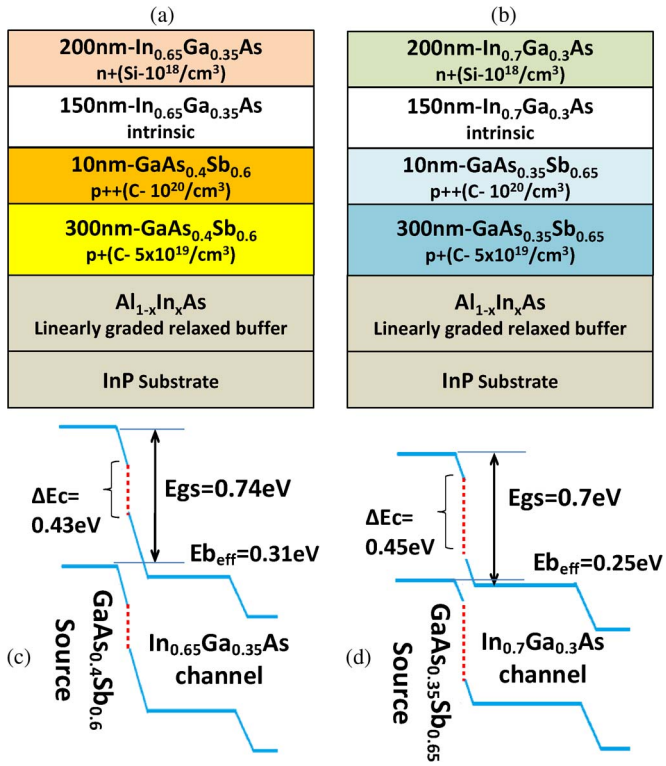

Fig. 1. (a) and (b) Cross-sectional schematics of (a) the $\rm GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ moderate hetj and (b) the $\rm GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ high hetj TFET layer structures. (c) and (d) Energy band diagrams showing the band alignment at the moderate- and high-stagger S–C heterointerface.

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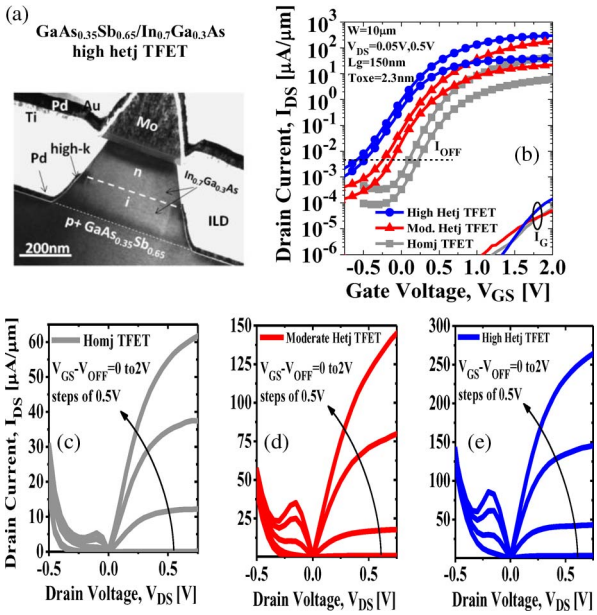

Fig. 2. (a) Cross-sectional TEM image of the fabricated nanopillar high hetj TFET device. (b) Measured room temperature transfer characteristics (I_{DS}–V_{GS}) of the $In_{0.7}Ga_{0.3}As$ homj TFET ($Eb_{eff} = 0.58$ eV), $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ moderate hetj TFET ($Eb_{eff} = 0.31$ eV), and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ high hetj TFET ($Eb_{eff} = 0.25$ eV). (c)–(e) Measured output characteristics (I_{DS}–V_{DS}) of the fabricated devices. I_{ON} increases by 253% due to a decrease in Eb_{eff} from 0.58 to 0.25 eV.

350%, exhibiting a record high I_{ON} of 135 μA/μm. Drain-induced barrier thinning (DIBT) is shown to reduce by 65% at $V_{DS} = 0.5$ V.

Section II describes the layer structure and device fabrication details; Section III discusses electrical results and benchmarks I_{ON} and I_{ON}/I_{OFF}; Section IV concludes this letter.

II. Layer Structures and Device Fabrication

$In_{0.7}Ga_{0.3}As$ homj control and $GaAs_{1-x}Sb_x/In_yGa_{1-y}As$ hetj TFETs with moderate ($x = 0.6,\ y = 0.65$) and high ($x = 0.65,\ y = 0.7$) stagger were grown on a semi-insulating InP substrate using solid-source molecular beam epitaxy. Fig. 1(a) and (b) shows the schematic layer structures for the hetj TFETs. The channel material consists of 150 nm of intrinsically doped $In_{0.7}Ga_{0.3}As$ for the high hetj TFET and 150 nm of $In_{0.65}Ga_{0.35}As$ for the moderate hetj TFET. The layer structure for the $In_{0.7}Ga_{0.3}As$ homj TFET is essentially the same as the high hetj TFET, except that the $GaAs_{0.35}Sb_{65}$ source region is replaced by $In_{0.7}Ga_{0.3}As$. Fig. 1(c) and (d) shows the energy band diagrams explaining the band alignment for the moderate and high hetj TFETs at the staggered source–channel (S–C) interface. Eb_{eff} is approximately given by $E_{gs} - \Delta E_C$, where E_{gs} is the band gap of the source, and ΔE_C represents the conduction band discontinuity [6].

Fig. 2(a) shows the cross-sectional transmission electron microscopy (TEM) image of the fabricated vertical nanopillar high hetj TFET device. The detailed nanopillar TFET fabrication process flow can be referred in [7]. The high-k stack consists of 1-nm Al_2O_3/3.5-nm HfO_2 (Toxe = 2.3 nm) grown by an atomic layer deposition technique at 250 °C. The gate metal on the pillar sidewall consists of 20-nm electron-beam evaporated Pd.

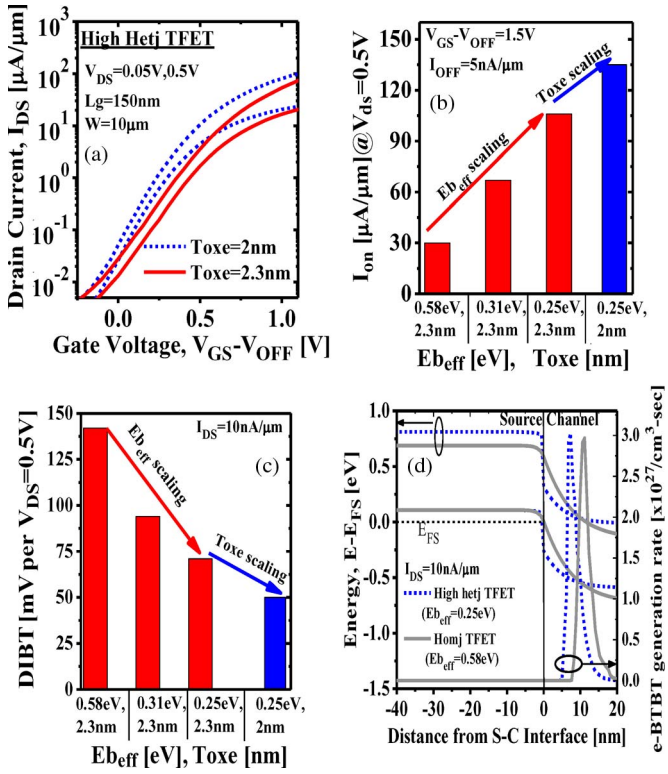

Fig. 3. (a) Reduction in the SS of the I_{DS}–V_{GS} of the high hetj TFET due to scaling of Toxe from 2.3 to 2 nm. (b) and (c) Histograms summarizing enhancement in I_{ON} and reduction in DIBT by scaling Eb_{eff} and Toxe. (d) Simulations showing the comparison of electron band-to-band tunneling (e-BTBT) generation profiles between the homj and high hetj TFETs at 10 nA/μm, $V_{DS} = 0.5$ V [8]. With reducing Eb_{eff} due to increasing stagger, BTBT generation occurs closer to the metallurgical S–C interface.

III. Electrical Results and Benchmarking

Fig. 2(b) shows room temperature transfer characteristics (I_{DS}–V_{GS}) of the homj TFET and moderate and high hetj TFET devices measured at $V_{DS} = 0.05$ and 0.5 V. It can be observed that turnoff voltage V_{OFF} shifts left with reducing Eb_{eff}. This is expected since, with higher ΔE_C and a lower Eb_{eff}, the same tunneling current can be achieved at a lower applied gate bias. At $I_{OFF} = 5$ nA/μm, $V_{DS} = 0.5$ V, $V_{GS} - V_{OFF} = 1.5$ V, and Toxe = 2.3 nm, the high hetj TFET exhibits $I_{ON} = 106$ μA/μm, which shows that band-gap engineering can fundamentally mitigate the drive current limitation in TFETs. Fig. 2(c)–(e) shows the room temperature output characteristics (I_{DS}–V_{DS}) for the different TFET devices. All devices show clear signature of output drain-current saturation. The negative differential resistance behavior observed for negative V_{DS} is a characteristic behavior of an Esaki tunneling junction.

Fig. 3(a) compares I_{DS}–V_{GS} of the high hetj TFET device with Toxe = 2 and 2.3 nm. Fig. 3(b) summarizes the enhancement in I_{ON} as a result of Eb_{eff} and Toxe scaling. With Toxe being 2.3 nm and Eb_{eff} scaled from 0.58 eV (homj TFET) to 0.31 eV (moderate hetj TFET), the I_{ON} at $V_{DS} = 0.5$ V and $V_{GS} - V_{OFF} = 1.5$ V increases by 123%. With further reduction in Eb_{eff} to 0.25 eV (high hetj TFET), the enhancement increases to 253% primarily due to increased tunneling transmission efficiency. By scaling Toxe to 2 nm in conjunction, the high hetj TFET exhibits $I_{ON} = 135$ μA/μm (350% enhancement over the homj TFET) at $V_{DS} = 0.5$ V and $V_{GS} - V_{OFF} = 1.5$ V. This is the highest ever gated interband tunneling

TABLE I
BENCHMARKING OF THE HIGH HETJ TFET I_{ON} AGAINST THOSE EXPERIMENTALLY DEMONSTRATED TO DATE. THE HIGH HETJ TFET SHOWS NOT ONLY THE HIGHEST I_{ON} BUT ALSO THE HIGHEST I_{ON}/I_{OFF} AT $I_{ON} = 135\ \mu A/\mu m$, $V_{DS} = 0.5$ V

Reference	Eb_{eff} (eV)	Lg (nm)	Toxe (nm)	V_{GS}-V_{OFF} (V)	V_{DS} (V)	I_{ON} (μA/μm)	I_{ON}/I_{OFF}	SS_{eff} (mV/dec)
Dewey et. al IEDM, 2011 [2]	0.74	100	1.1	0.9	0.3	8	$1.6x10^3$	140
Dewey et. al IEDM,2011 [2]	0.58	100	1.1	0.9	0.3	17	$3.4x10^3$	106
Zhao et. al, EDL, 2011 [11]	0.58	100	1.2	1.5	0.5	30	$6x10^3$	200
Mohata et. al IEDM, 2011 [12]	0.25	150	2.3	1.5	0.5	135	10	750
(This work) Homj	0.58	150	2.3	1.5	0.5	30	$6x10^3$	200
(This work) Mod. Hetj	0.31	150	2	1.5	0.5	78	$1.5x10^4$	179
(This work) High Hetj	0.25	150	2	1.5	0.5	135	$2.7x10^4$	169

current reported to date at $V_{DS} = 0.5$ V. Fig. 3(c) plots DIBT, calculated at $I_{DS} = 10\ nA/\mu m$ and $V_{DS} = 0.5$ V. Due to Eb_{eff} and Toxe scaling, DIBT reduces by 65%. DIBT improves with reducing Eb_{eff} due to the interband generation occurring closer to the S–C metallurgical interface, thus improving device electrostatics, as shown in Fig. 3(d) [9]. I_{ON}/I_{OFF} is another key factor to consider. In this letter, Eb_{eff} has been reduced by 57% and could have been achieved in two ways: 1) by reducing the band gap in the homj TFET or 2) by modifying the stagger using band lineup engineering in the hetj TFET, as shown in this letter. In both cases, I_{OFF} will be determined by the Shockley–Read–Hall (SRH) generation-dominated leakage of a reversed biased p-i-n diode [10]. In the former case, a change in the homj band gap from 0.58 to 0.25 eV (57% decrease) would lead to an exponential increase in leakage by ∼570 times at room temperature. In the second case, the bulk SRH generation rate is expected to linearly change since the constituent band-gap values stay unchanged and only the built-in field at the tunnel junction changes. This explains why the leakage current changes only by three times and highlights the advantage in employing staggered heterojunctions to enhance drive currents in TFETs while maintaining similar ON–OFF current ratio. The SS in all the fabricated devices is greater than 60 mV/dec at room temperature due to the presence of high density of interface states D_{it} at the high-k/channel interface [13] and can be improved by including proper surface passivation and high-temperature anneal process steps. The modest degradation observed in the point SS with reducing Eb_{eff} is due to the factor of 3 increasing in the bulk leakage current [see Fig. 2(b)] and can be mitigated by scaling pillar thickness T_{body}.

Table I benchmarks the measured I_{ON} of the high hetj TFET against those experimentally demonstrated to date. The hetj TFET exhibits the highest $I_{ON} = 135\ \mu A/\mu m$ with the highest $I_{ON}/I_{OFF} = 2.7 \times 10^4$ ratio. This demonstration of I_{ON} exceeding 100 $\mu A/\mu m$ shows that, fundamentally, it is possible for TFETs to deliver MOSFET-like performance at low V_{CC} (≤0.5 V). In the fabricated devices, the device geometry has not been significantly scaled ($T_{body} =$ 500 nm, Toxe = 2 nm), and I_{DS} at $V_{GS} - V_{OFF} = 0.5$ V is only 10 $\mu A/\mu m$. Thus, the large overdrive voltage of $V_{GS} - V_{OFF} = 1.5$ V is required in order to benchmark the high I_{ON} demonstrated. Further scaling in device geometry and D_{it} will enable demonstration of the high I_{ON} within $V_{ON} - V_{OFF} = 0.5$ V. Finally, the effective SS, benchmarked as $SS_{eff} = (V_{TH} - V_{OFF})/(\log(I_{TH}/I_{OFF}))$ [14] between V_{OFF} and $V_{TH} = (V_{GS} + V_{OFF})/2$, reduces with decreasing Eb_{eff} and can be explained in line with the improvement in DIBT.

IV. CONCLUSION

$In_{0.7}Ga_{0.3}As$ homj control, $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ moderate-stagger, and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ high-stagger hetj TFETs have been fabricated, and the dependence of I_{ON} and DIBT (short-channel effect) on effective tunneling barrier height Eb_{eff} has been systematically studied. By scaling Eb_{eff} from 0.58 to 0.25 eV, 253% enhancement in I_{ON} is demonstrated at $V_{DS} = 0.5$ V, arising due to increased tunneling efficiency. Furthermore, using Toxe scaling in conjunction with Eb_{eff} engineering, a record high $I_{ON} = 135\ \mu A/\mu m$ (350% enhancement) along with the highest $I_{ON}/I_{OFF} = 2.7 \times 10^4$ in the category of TFETs is achieved at $V_{DS} = 0.5$ V and $V_{GS} - V_{OFF} = 1.5$ V. DIBT is shown to reduce by 65% due to the band-to-band generation occurring closer to the S–C interface, thus improving device electrostatics.

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