Review

Yan Zhu and Mantu K. Hudait*

Low-power tunnel field effect transistors using mixed As and Sb based heterostructures

Abstract: Reducing supply voltage is a promising way to address the power dissipation in nano-electronic circuits. However, the fundamental lower limit of sub-threshold slope (SS) within metal oxide semiconductor field effect transistors (MOSFETs) is a major obstacle to further scaling the operation voltage without degrading ON/OFF ratio in current integrated circuits. Tunnel field-effect transistors (TFETs) benefit from steep switching characteristics due to the quantum-mechanical tunneling injection of carriers from source to channel, rather than by conventional thermionic emission in MOSFETs. TFETs based on group III-V compound semiconductor materials further improve the ON-state current and reduce SS due to the low band gap energies and smaller carrier tunneling mass. The mixed arsenide/antimonide (As/Sb) \( \text{In}_{x}\text{Ga}_{1-x}\text{As/ GaAs}_{y}\text{Sb}_{1-y} \) heterostructures allow a wide range of band gap energies and various staggered band alignments depending on the alloy compositions in the source and channel materials. Band alignments at source/channel heterointerface can be well modulated by carefully controlling the compositions of the mixed As/Sb material system. In particular, this review introduces and summarizes the progress in the development and optimization of low-power TFETs using mixed As/Sb based heterostructures including basic working principles, design considerations, material growth, interface engineering, material characterization, device fabrication, device performance investigation, band alignment determination, and high temperature reliability. A review of TFETs using mixed As/Sb based heterostructures shows superior structural properties and distinguished device performance, both of which indicate the mixed As/Sb staggered gap TFET as a promising option for high-performance, low-standby power, and energy-efficient logic circuit application.

Keywords: mixed As and Sb based heterostructures; staggered gap band alignment; tunnel field effect transistors (TFETs).

*Corresponding author: Mantu K. Hudait, Advanced Devices and Sustainable Energy Laboratory (ADSEL), Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, USA, e-mail: mantu@vt.edu

Yan Zhu: Advanced Devices and Sustainable Energy Laboratory (ADSEL), Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, USA

1 Introduction

The dimension of silicon (Si) metal oxide semiconductor field effect transistors (MOSFETs) has been scaled by three orders of magnitude in the past decades in order to achieve low-power, high-performance devices and integrated circuits. Extraordinary improvements have been achieved in switching speed, device density, functionality, and cost of microprocessors due to the downsampling of device geometry. However, further downsampling of conventional Si MOSFETs faces critical issues: the increasing difficulty in further reducing the supply voltage, and the increasing leakage current that degrades the switching current ratio between ON and OFF states \( (I_{ON}/I_{OFF}) \) ratio, both of which will result in high power consumption. As can be seen from Figure 1 [1], which is a plot of active power density (blue line) and subthreshold power density (red line) from commercial Si MOSFETs, the leakage power starts to dominate in advanced transistor as scaling of gate length. The leakage power density will exceed the active power density if the gate length is below the cross point of these two lines as labeled in Figure 1. Besides, as the transistor gate length is reduced, supply voltage \( (V_{dd}) \) should be lowered to keep high device performance and reduce power dissipation. To meet the \( I_{on} \) requirements, the threshold voltage \( V_{th} \) needs to be scaled with \( V_{dd} \). However, for Si MOSFETs, \( I_{off} \) exponentially increases with \( V_{th} \) reduction and is given by [2]:

\[
I_{off} = I_{ds} \cdot 10^{rac{V_{th}}{SS}}
\]

(1)

where \( I_{ds} \) is the drain to source current and SS is the sub-threshold slope (also be referred to as inverse subthreshold
slope in the literature) of the device which is the change of gate voltage, $V_{gs}$, that must be applied to create one decade increase in the output current or as defined as [3]:

$$SS = \frac{dV_{gs}}{d\log I_{ds}} \text{[mV/dec]}$$  \hspace{1cm} (2)$$

For the conventional MOSFET, the subthreshold current is the diffusion current and SS is independent of $V_{gs}$ and is given by [4]:

$$SS = \frac{kT}{q} \ln 10 \left(1 + \frac{C_{dm}}{C_{ox}}\right).$$  \hspace{1cm} (3)$$

where, $kT/q$ is the thermal factor, $C_{dm}$ is the depletion capacitance, and $C_{ox}$ is the gate oxide capacitance. Eq. (3) approaches a well-known lower limit of approximately 60 mV/dec at $T=300$ K when $C_{dm}/C_{ox}$ is close to zero. But in practice, caused by the short-channel effects (SCEs), SS is far worse than an ideal value of 60 mV/dec [1, 5]. The change of transfer characteristics ($I_{ds}$ vs. $V_{gs}$) of a MOSFET as the scaling of $V_{th}$ is shown in Figure 2 (black lines). It can be seen from Figure 2 that MOSFET shows an exponential increase in $I_{off}$ due to the incompressible lower limit of SS. As demonstrated in Eq. (1), to lower $V_{th}$ without the degradation (increasing $I_{off}$) of transistor performance, transistor with a steep SS, called steep slope switches (SSS, as shown in the green line in Figure 2) are expected to reduce both ON-state and OFF-state power consumption.

Recently, tunnel field effect transistors (TFETs) [6–15] based on the band-to-band tunneling (BTBT) injection mechanism have been proposed as one of SSS to replace MOSFET for low-power applications. TFETs have advantages over conventional MOSFETs in terms of lower $I_{off}$ and steeper SS [9, 10, 16]. To design a TFET with high performances, a proper material system needs to be selected. Among all material systems, III-V heterostructures can provide a smaller effective tunneling mass [5, 15, 17] and allow different band alignments between the source/channel tunnel junction [5–15] for the enhancement of $I_{on}$ and reduction of $I_{off}$. Among them, mixed As/Sb based heterostructures [9, 11–15], namely, GaAs$_{y}$Sb$_{1-y}$/In$_x$Ga$_{(1-x)}$As provide a wide range of band gaps and band alignments depending on the alloy compositions in the source and

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**Figure 1** Power density of the active region (blue line) and subthreshold region (red line) from commercial Si MOSFETs. The subthreshold power density takes more and more proportion of the total power consumption with the scaling of gate length. The subthreshold leakage power density will be higher than the active power density if the gate length is below the cross point of these two lines as labeled in the figure. Reprinted from Ref. [1], with permission, from IBM Technical Journals.

**Figure 2** Comparison of the transfer characteristics ($I_{ds}$ vs. $V_{gs}$) of ideal transistors (orange line), MOSFETs (black lines), and steep slope switches (SSS, green line). Owing to the incompressible 60 mV/dec SS at 300 K for MOSFETs, $I_{off}$ of MOSFETs shows exponential increase with the scaling of $V_{th}$.
channel materials [11–15]. As a result, the band offset of source/channel junction can be well modulated to guarantee high $I_{on}$ without sacrificing $I_{off}$ by properly selecting the material compositions in source and channel regions. Therefore, the mixed As/Sb material system has been proposed as a promising candidate for high-performance TFET application. In this review, the operating principle, design, and optimization of TFETs are reviewed. We concentrate on the mixed As/Sb TFETs and discuss the advantages and application potential of these structures and devices. The latest simulation results and experimental data relating to these structures and devices are reported. The key design parameters as well as the critical characteristics relating to both the structural stability and the device reliability are systematically investigated. Finally, prospects of the mixed As/Sb TFETs for further performance improvement and future integration on Si substrates are also discussed.

2 Fundamental operating principles of TFETs

2.1 Basic working principles

The TFET is a gated p'-i-n' diode with a gate over the intrinsic region. The gated p'-i-n' diode is always reverse-biased to obtain ultra-low leakage current. A schematic cross-section of an n-type TFET device with applied source ($V_s$), gate ($V_{gs}$), and drain ($V_{ds}$) voltages is shown in Figure 3A [4, 18]. For an n-type TFET, the heavily p-type doped region is called the source, the intrinsic region is called the channel, and the heavily n-type doped region is called the drain. When a positive voltage is applied to the heavily n-type doped region, the p'-i-n' diode is reverse-biased and ready to be switched by the gate. The schematic band diagrams of the TFET device on the OFF-state is shown by red lines in Figure 3B [4, 18]. As shown in Figure 3B, under zero gate-source bias voltage ($V_{gs}$=0), the BTBT process is suppressed due to the gap between the source valence band maximum and the channel conduction minimum (and the resulting lack of available states with appropriate energy within the channel conduction band to accept tunneling electrons). When a TFET is on OFF-state, only p'-i-n' diode leakage current flows between the source and drain, and this current can be extremely low. By contrast, the band diagram of the n-type TFET on the ON-state is shown by green lines in Figure 3B [4, 18]. With positive $V_{gs}$, the energy bands of the intrinsic channel region are pushed down by $q\Delta V_{gs}$ as labeled in Figure 3B [4, 18]. With increasing $V_{gs}$, the channel conduction band minimum was pushed below the source valence band maximum. As a result, the tunneling barrier width (labeled as $\lambda$ in Figure 3B) [4, 18]) between the p-type source and intrinsic channel is significantly reduced (less than 10 nm). The reduced tunneling barrier enables a significant amount of electrons tunnel from occupied states in the source valence band to unoccupied states in the channel conduction band with the same energy alignment in an energy window of $\Delta \Phi$ as labeled in Figure 3B [4, 16, 18] and these tunneling electrons will finally be collected by the drain.

In principle, the TFET is an ambipolar device with symmetry between the n-type and p-type sides (similar doping levels, similar gate alignment, etc.), showing n-type behavior with dominant electron conduction and p-type behavior with dominant hole conduction. The band diagram of the same structure as shown in Figure 3A working as a p-type TFET is shown in Figure 3C [4, 18]. For a p-type TFET, the heavily n-type doped region is called the source, the intrinsic region is called the channel, and the heavily p-type doped region is called the drain. As shown in red lines in Figure 3C [4, 18], the OFF-state band diagram of a p-type TFET is the same as that for an n-type TFET. No conduction is taking place in the TFET without

![Figure 3](image-url)
gate bias due to the valence band maximum of the intrinsic channel located below the conduction band minimum of the n-type source. The BTBT process is suppressed, leading to very small OFF-state leakage current which is dictated by the reverse-biased p⁺-i-n⁺ diode. By applying a negative gate voltage, the energy bands of the channel were pulled up as shown in green lines in Figure 3C [4, 18]. A conductive channel opens as soon as the channel valence band maximum is lifted above the source conduction band minimum because holes in the source conduction band can tunnel into empty states of the channel valence band (or it can also be described as electrons in the channel valence band can tunnel into empty states of the source conduction band) [4]. The tunneling holes are finally collected by the p-type drain.

2.2 ON-state current

The $I_{ON}$ of a TFET depends on the tunneling probability of the BTBT process [18]. The tunneling barrier for TFETs can be approximated by a triangular potential [4], as indicated in the blue shading in Figure 3B and C [4, 18], and the tunneling probability can be calculated using WKB (Wentzel-Kramers-Brillouin) approximation [19, 20]:

$$T_{WKB} = \exp \left[ -2 \int_0^w |k(x)| \, dx \right].$$

where $|k(x)|$ is the absolute value of the wave vector of the carrier inside the barrier. $x=0$ and $x=w$ are the classical boundaries of triangular potential shown in Figure 4 [19]. The wave vector inside a triangular barrier can be expressed from the $E$-$k$ relationship [19]:

$$k(x) = \sqrt{\frac{2m^*(V-E_c)}{\hbar^2}}$$

where $V$ is the potential energy. For tunneling consideration, the incoming electron has a potential energy equal to the bottom of the energy gap and the varying conduction-band edge $E_c$ can be expressed in terms of the electric field $E$ as a function of $x$. Thus, the wave vector inside the triangular barrier is given by [19]:

$$k(x) = \sqrt{\frac{2m^*(-qEx)}{\hbar^2}}.$$  \hspace{1cm} (6)

Substituting Eq. (6) into Eq. (4) yields [19]:

$$T_{WKB} = \exp \left[ -2 \int_0^w \left( \frac{2m^*(-qEx)}{\hbar^2} \right) \, dx \right].$$

For a triangular barrier as shown in Figure 4 [19] with a uniform electric field, $w=E_c/E_0$, so [19]:

$$T_{WKB} = \exp \left[ -4 \sqrt{\frac{2m^*E_g^{3/2}}{3q\hbar E}} \right].$$

Eq. (8) is a general expression for BTBT transmission probability. This equation can be improved by making it more specific for TFETs. Now comparing Figure 4 to the TFET band diagrams shown in Figure 3B and C [4, 18], it can be found that the height of the triangular barrier is $\Delta \Phi+E_0$, and the tunneling barrier width is $\lambda$. Here, $\Delta \Phi$ is the energy window over which tunneling can take place. As a result, the electric field in Eq. (8) can be expressed as, $E=(\Delta \Phi+E_0)/\lambda$. Eq. (8) can be rewired as:

$$T_{WKB} = \exp \left[ -4 \lambda \sqrt{\frac{2m^*E_g^{3/2}}{3q\hbar(\Delta \Phi+E_0)}} \right].$$

Here, $m^*$ is the effective mass and $E_c$ is the band gap. On the basis of the triangular barrier approximation discussed above, $\Delta \Phi+E_0$ is the triangular barrier height for carriers to tunnel from source to channel. As shown in Figure 3B, for an n-type TFET, the triangular barrier was denoted as blue shading and $E_0$ corresponds to the band gap energy of source material. The triangular barrier for a p-type TFET is also shown as blue shading in Figure 3C.
Different as the case with n-type TFET, $E_g$ corresponds to the band gap energy of channel material for a p-type TFET [4, 18]. There are four important requirements in order for BTBT to take place: available states in the source to tunnel from, available state in the channel to tunnel into, a tunneling barrier width that is narrow enough for tunneling through, and the conservation of momentum [21].

For indirect semiconductor materials such as Si, crystal phonons are necessary to conserve momentum to assist the tunneling process. In that case, $E_g$ in the numerator of Eq. (9) should be replaced by $E_g - E_P$, where $E_P$ is the phonon energy [21] and the effective mass $m^*$ should be changed to $m^*_P$, which is the reduced effective mass in the tunneling direction. If these changes are not made in Eq. (9), the BTBT current will be overestimated for indirect materials. A higher BTBT current can be expected if $m^*$ and $\lambda$ can be made as small as possible. In principle, a reduction of $E_g$ can also increase the tunneling probability. However, a small energy band gap will lead to an increase of $I_{OFF}$ due to thermal emission becoming more pronounced [18], and as a result a proper $E_g$ should be selected to meet a desired $I_{OFF}/I_{ON}$ ratio.

### 2.3 OFF-state leakage

For an ideal TFET at OFF-state, the leakage current is only the p'-i-n' leakage current flows between the source and the drain. This leakage current can be extremely low and less than a fA/µm as indicated by simulation [21]. However, in practice, there are five primary leakage mechanisms contributing to the OFF-state leakage of TFET [22]: (i) gate leakage through the high-κ gate dielectric; (ii) thermionic emission over the source-drain built-in potential (the p'-i-n' diode leakage current as we mentioned above); (iii) Shockley-Read-Hall generation-recombination (SRH G-R) in the heavily doped source and drain depletion regions; (iv) direct tunneling and defect-assisted tunneling process; and (v) ambipolar conduction. As the first two are well known, the other three mechanisms are explained below.

The SRH G-R mechanism is illustrated in Figure 5A [22]. The SRH G-R current is a common leakage current component especially in III-V material based TFETs due to the low-band gap energy of these materials [9–11, 15, 23, 24]. The most obvious feature of the SRH G-R dominated $I_{OFF}$ is its strong temperature dependence [11, 23, 24]. The main contribution to the temperature dependence of the SRH G-R mechanism arises from the intrinsic carrier concentration $n_i$, which is proportional to $\exp(-E_g/2kT)$, where $E_g$ is the band gap energy, $k$ is the Boltzmann constant, and $T$ is temperature [23]. TFETs with a SRH G-R dominated leakage current usually show an activation energy ($E_a$) approximately half of $E_g$ [23, 24]. As the SRH G-R current increases exponentially with temperature, the SRH G-R dominated leakage will deteriorate the performance of TFET devices at high temperature. Experimental results showed that the SRH G-R current increased by three orders from 25°C to 150°C in an In$_{0.7}$Ga$_{0.3}$As/GaAs$_{0.35}$Sb$_{0.65}$ n-type TFET [24], which in turn reduced the $I_{OFF}/I_{ON}$ ratio by several orders.

Another leakage mechanism for TFET is the tunneling leakage current, including both direct BTBT and the defect-assisted tunneling. With the scaling of gate lengths, direct BTBT as well as defect-assisted tunneling become dominate especially for narrow band gap channels such as InAs [25] and for graphene nanoribbon [26]. Figure 5B [22] shows the band diagrams of this leakage mechanism. It should be noted that the direct BTBT mechanism will dominate the OFF-state transport of some heterostructure TFETs even with a high gate length [11, 13]. High defect density at the source/channel heterointerface will introduce fixed positive charges, which will change the band alignment of the source/channel material at the interface and assist the band line-up transition from a staggered gap to broken gap. Thus, this broken gap band alignment caused by high-defect density will enable BTBT transport even at OFF-state [11, 13]. This defect-assisted band alignment transition will be discussed in detail in Section 4.6.

Besides, the ambipolar current as illustrated in Figure 5C [22] can also contribute to the OFF-state leakage of TFETs. As discussed in Section 2.1, the TFET is an ambipolar device if the n-type and p-type regions are symmetric. If a negative bias is applied to the gate of an n-type TFET, the energy bands of the channel will be lifted up. If the negative gate bias is large enough to pull the channel valence band
maximum above the drain conduction band minimum as shown in Figure 5C [22], reverse tunneling at the drain can inject minority carriers into the channel that leads to an ambipolar leakage. Ways to suppress this ambipolar leakage of TFETs will be discussed in detail in Section 2.5.

2.4 Subthreshold slope

The SS of a TFET without a lower limit is one of the key advantages over traditional MOSFET. As can be seen from Figure 3B and C, due to the band gap of source material, the low energy tail of Fermi distribution is cut off in the source side. The channel also cuts off the high energy part of the Fermi distribution such that the tunnel junction acts as a band-pass filter allowing only carriers in the energy window $\Delta \Phi$ to tunnel into the channel [18]. Thus, the electronic system is effectively “cooled down”, behaving as a conventional MOSFET at a lower temperature. This filtering function makes it possible to achieve an SS lower than 60 mV/dec at 300 K [4].

The definition of SS is demonstrated in Eq. (2). To derive an expression of the SS for a BTBT device, the expression for the tunneling current through a reverse-biased p-n junction can be used [19, 21, 27]:

$$I = aV_{gs}E \exp\left(\frac{b}{E}\right)$$

(10)

where $V_{eff}$ is the tunnel junction bias as shown in the inset of Figure 6A [27], $E$ is the electric field, and $a$ and $b$ are coefficients determined by the material properties of the junction and the cross-sectional area of the device [22, 27]. Specifically

$$a = \frac{Aq^3}{4\pi^2 \hbar^2}$$

(11)

and

$$b = \frac{4\sqrt{\pi}E_g^{2/3}}{3q\hbar^2}.$$  (12)

Using the definition of SS from Eq. (2), the SS of TFET can be described as:

$$SS = \ln 10 \frac{dV_{gs}}{dV_{DD}} + E + \frac{b}{E} \frac{dV_{gs}}{dV_{DD}}.$$  (13)

From Eq. (13), it can be found that there are two terms involved to determine the SS of a TFET device and these terms are not limited to $kT/q$ [22, 27]. The first term reflects the control of gate bias ($V_{gs}$) to the tunnel junction bias ($V_{eff}$). As a result, the transistor should be engineered so that the $V_{gs}$ can directly and efficiently control $V_{eff}$, which suggests that a transistor with a thin geometry and/or high-$\kappa$ gate dielectric is desired to make sure that the gate
bias can directly modulate the channel [27]. For an equivalent oxide thickness (EOT) approaching 1 nm, \( \frac{dV_{\text{eff}}}{dV_{\text{GS}}} = 1 \) and the first term of Eq. (13) is approximately inversely related to \( V_{\text{gs}} \). As a result, the SS of TFET increases with \( V_{\text{gs}} \), which is a main difference of TFET from MOSFET and this changing trend is illustrated in Figure 6A [21] with different gate dielectrics. Therefore, if the transfer characteristics \((I_{\text{ds}}, V_{\text{gs}})\) of a TFET is plotted with \( I_{\text{ds}} \) in a log scale, the subthreshold region of TFET does not appear as a straight line as that of MOSFET [21]. This difference is clearly shown in Figure 6B [28] by comparing the transfer characteristics of a typical MOSFET and a typical TFET. The SS of TFET is smallest at the lowest \( V_{\text{gs}} \), and increases with \( V_{\text{gs}} \). These characteristics of TFET have been observed both in experiments [6] and simulations [29, 30]. By contrast, the SS can be minimized by maximizing the second term of Eq. (13). This occurs if the gate is placed in a proper direction to align the applied gate electric field with the internal electric field of the tunnel junction. In this way, the gate electric field adds to the internal electric field and the tunneling probability was enhanced [22].

Owing to the strong dependence of SS on \( V_{\text{gs}} \), it is useful to define two different types of SS, point SS (SS\(_{\text{pt}}\)) and average SS (SS\(_{\text{avg}}\)) (the latter one is more important for switching properties) [2]. The inset of Figure 6B [2, 21] shows these two SS types. Point SS is the smallest value of the SS on the \( I_{\text{ds}}, V_{\text{gs}} \) curve, typically found just as the device leaves its OFF-state and tunneling current starts to flow. Average SS is taken from the point where the device starts to be turned ON, up to \( V_{\text{th}} \) [21, 22, 31]. The average SS can be expressed as:

\[
SS_{\text{avg}} = \frac{V_{\text{th}} - V_{\text{off}}}{\log \left( \frac{I_{\text{on}}}{I_{\text{off}}} \right)}.
\]

### 2.5 Approaches to reduce ambipolar behavior

As discussed in Section 2.1, the TFET is an ambipolar device if the n\(^+\) region and the p\(^+\) region are symmetric in geometry and doping concentration, which shows n-type tunneling properties with positive gate bias but shows p-type tunneling properties with negative gate bias. As a result, the ambipolar properties result in similar transfer characteristics with positive and negative gate biases, as shown in Figure 7 [32], leading to parasitic conduction at OFF-state. Therefore, different methods should be used to reduce the ambipolar behavior of TFET.

For an n-type TFET, the device is turned on by applying positive gate bias, which creates an n\(^+\) inversion layer underneath the gate. With increasing gate voltage, electron concentration in the n\(^+\) inversion layer increases, thereby decreasing the p\(^-\)n\(^+\) tunneling barrier width \( \lambda \) at the source side. The reduction of this tunneling barrier width directly results in an increase of \( I_{\text{off}} \) as long as the dominant resistance between the source and drain is formed by this tunneling barrier, which means that the channel resistance is only a small fraction of the tunneling barrier resistance. Furthermore, the tunneling barrier width is determined by the carrier concentration in the n\(^+\) layer close to the source region. As a result, it is possible to create a high-resistance region in the channel near the drain without affecting \( I_{\text{on}} \) of the TFET [33]. This high-resistance region near the drain can effectively block the ambipolar tunneling if a negative gate bias is applied. On the basis of this consideration, TFET devices without gate-drain overlap were proposed to reduce the ambipolar behavior [33]. The schematic cross-section of this TFET device is shown in Figure 8A [33], and the simulated transfer characteristics of TFET devices with and without gate-drain overlap are compared in Figure 8B [33]. It can be seen from Figure 8B that with similar doping levels in the source and drain, the TFET with gate-drain overlap is ambipolar, whereas the \( I_{\text{off}} \) of the TFET without gate-drain overlap remains low, which is due to the high-resistance region in the channel near the drain. In the TFET without gate-drain overlap, the large carrier density build-up by
negative gate bias in the gated channel region no longer extends to the drain, leaving an area with low hole concentration adjacent to the drain/channel junction. In addition, owing to the reduced inversion carrier concentration near the drain, the built-in electrical field at the drain/channel junction was reduced. As a result, tunneling of holes from the drain to the channel at the drain/channel junction with a negative gate bias is reduced and the OFF-state condition of the device can be controlled properly [33]. Similar approaches to reduce the ambipolar properties are also achieved by other researchers [32, 34], all of which illustrated significant reduction of ambipolar current using this method.

Another approach of reducing ambipolar current of TFET is to lower the doping concentration of the drain region, which can increase the tunneling barrier width for holes at the channel/drain interface due to the enlarged tunneling barrier width at a lower doping concentration [34]. For n-type TFET, the p-type tunneling between the channel and drain is significantly suppressed, because tunneling current decreases exponentially with increasing tunneling barrier width. By contrast, the $I_{ON}$ is controlled by the electron BTBT from source to channel, so it is insensitive to the drain doping concentration. As a result, asymmetric source-drain doping offers a successful scheme for suppressing the ambipolar characteristics of TFETs [34]. As shown in Figure 9, by reducing the drain side doping concentration, the BTBT from the drain to the channel was significantly suppressed and the ambipolar current was reduced by several orders of magnitude [34]. Actually, both of these approaches, by reducing channel-drain overlap or decreasing drain doping concentration, are not fundamentally different and both suppress the ambipolar current by introducing a long depletion width and low electric field on the drain side [32]. As a result, a combination of these two methods can further reduce the ambipolar current of TFETs.

### 3 Key considerations for design of TFETs

#### 3.1 Band alignments and effective tunneling barrier height

Based on different band alignment types of the source/channel materials, TFETs can be classified to (i) homojunction, (ii) staggered gap, and (iii) broken gap structures. The schematic band diagrams of these three types of TFETs at ON-state are shown in Figure 10A–C, respectively. For a homojunction TFET, the same material was used in both source and channel regions and the tunnel junction is formed by the heavy doping concentration in the source side. As a result, the sharpness of the doping profile at the tunnel junction is critical for a homojunction TFET, as it determines the tunneling barrier width ($\lambda$) of carrier from source to the channel. A major drawback of homojunction TFETs is the lack of high $I_{ON}$ [35] due to the relatively larger tunneling barrier width ($\lambda$). By taking advantage of band alignments in heterojunction transistors, this figure of merit can be drastically improved, as predicted theoretically [36]. Some heterostructures offer a staggered band alignment, allowing a steeper band
structure profile over the junction than the homojunction, which is achievable only by using doping modulation [37]. As shown in Figure 10B, the staggered gap TFET is formed by two different materials with a type-II band alignment (e.g., In$_{x}$Ga$_{1-x}$As/GaAs$_{y}$Sb$_{1-y}$) at the source/channel interface. Compared with the homojunction as shown in Figure 10A, the tunneling barrier width ($\lambda$) is reduced in the staggered gap TFET, resulting in higher $I_{ON}$ [9, 15]. A broken gap TFET is formed by a type-III heterointerface (e.g., InAs/GaSb) at the source/channel interface, which further reduced the tunneling barrier width ($\lambda$) leading to even higher $I_{ON}$.

An important parameter for designing a TFET device is the effective tunneling barrier height ($E_{eff}$), which is defined as the energy difference between the channel conduction band minimum and the source valence band maximum for an n-type TFET, but the energy difference between the source conduction band minimum and the channel valence band maximum for a p-type TFET, as shown in Figure 3B and C, respectively. This $E_{eff}$ plays a significant role on the performance of a TFET device, which not only determines the ON-state tunneling current but also sets the blocking barrier for OFF-state leakage.
[13]. For homojunction and staggered gap TFETs, the $E_{\text{beff}}$ is a positive value. The advantage of the staggered gap TFET is that the $E_{\text{beff}}$ can be well modulated by changing the material compositions on both source/channel sides. As a result, a tailored-made $E_{\text{beff}}$ can be achieved in a staggered gap TFET to boost $I_{\text{on}}$ without sacrificing $I_{\text{off}}$. In principle, a lower $E_{\text{beff}}$ is always preferred in designing TFET structures so that more tunneling carriers can be generated under the same gate bias, which in turn leads to a higher $I_{\text{on}}$. Experiments have already proved that by reducing $E_{\text{beff}}$ from 0.5 eV to 0.25 eV results in at least 200% improvement of $I_{\text{on}}$ in mixed As/Sb heterojunction TFETs due to the increase of tunneling transmission coefficient [9, 14]. However, if $E_{\text{beff}}$ is scaled to a negative value ($E_{\text{beff}}<0$), a broken gap band alignment will be formed at the source/channel interface. Although further improvement is expected on $I_{\text{on}}$ for a broken gap TFET due to the removal of tunneling barrier, $I_{\text{off}}$ will increase simultaneously and thus additional gate bias is required to turn off this tunneling mechanism [38]. As a result, for a broken gap TFET with negative $E_{\text{beff}}$, direct tunneling is taking place even without gate bias and an extra gate bias (negative for n-type and positive for p-type) is needed to turn this type of device OFF.

3.2 Doping levels and band gaps of source, channel, and drain

The doping levels of TFET source, channel, and drain must be carefully optimized to maximize $I_{\text{on}}$ and minimize $I_{\text{off}}$ [21]. In principle, the source region must be heavily and abruptly doped to boost $I_{\text{on}}$. Dopant abruptness less than 4 nm/dec is necessary to maximize the junction electric field that enables high $I_{\text{on}}$ [22]. This common practice, however, has some trade-offs to $I_{\text{on}}$ and SS if the source doping concentration is too high. As shown in Figure 11A for an n-type TFET, the source region is highly degenerated due to heavily p-type doping, which results in the source Fermi level $E_{\text{FS}}$ lying below the valence band maximum $E_v$. At a given temperature, electrons will partially occupy the states in the valence band between $E_v$ and $E_{\text{FS}}$ according to the Fermi Dirac distribution. Although a gate bias is applied, channel conduction band states will firstly be paired with source valence band electrons whose energy is between $E_v$ and $E_{\text{FS}}$ [39]. However, owing to high degenerate source material, these states are only partially occupied, which results in a reduced fraction of paired tunneling states to contribute to the conduction and thus degrades $I_{\text{on}}$. By contrast, to achieve higher efficiency of turn-on, which relates to steeper SS, every paired source valence band and channel conduction band states should be utilized to transport electrons via BTBT [39]. As a result, the high degenerate source material also degrades SS due to less available electrons in the source valence band within the energy window $\Delta \Phi$, as shown in Figure 11A. By contrast, a TFET structure with a lower doped source region demonstrates an $E_{\text{FS}}$ closer to $E_v$ in Figure 11B. In this case, a majority of the source valence band states are occupied, providing ample supply of electrons to contribute to tunneling when paired up states are available [22, 39], resulting in steeper SS and higher $I_{\text{on}}$ at lower $V_{\text{GS}}$.

Despite the degradation of SS and $I_{\text{on}}$, the highly degenerate source also increases OFF-state leakage due to the tunneling process via band tail states [37, 40]. The band tails caused by heavy doping decay exponentially [41–43] into the band gap as: $e^{-|E-E_{\text{FS}}|/E_T}$, where $E_T$ is the conduction (valence) band edge and $E_T$ is the Urbach parameter which can be comparable to room temperature.

![Figure 11](image-url) (A) Schematic band diagram of inefficient turn-ON of an n-type TFET device if the source region is highly degenerated. Energy states in the source valence band in the energy window $\Delta \Phi$ is only partially occupied according to Fermi Daric distribution, resulting in reduced $I_{\text{on}}$ and degraded SS. Reprinted, with permission, from Ref. [39] from IEEE. (B) Schematic band diagram of a TFET structure with a lower doped source. A majority of the source valence band energy states are occupied, providing ample supply of electrons to contribute to tunneling when paired up states are available, resulting in steeper SS and higher $I_{\text{on}}$ at lower $V_{\text{GS}}$. 
thermal energy, $k_B T = 26$ meV [40]. The band tails extend density of states into the band gap, which gives rise to the enhancement of tunneling from band tail states to the channel at OFF-state, resulting in a further increase of $I_{OFF}$. Besides, the energy states from band tails extending into the band gap reduce the energy difference between these states and the mid-gap traps, which in turn enhance SRH G-R leakage at OFF-state [40]. Nevertheless, although an overdoped source region can degrade SS, $I_{ON}$ and $I_{OFF}$ it is not desirable to introduce a lightly doped source in TFET structures, which reduces the electric field at the tunnel junction and increases excessive series resistance. A possible compromise may introduce moderately heavily doped pocket layer only adjacent to the tunnel junction and keep the other region of the source at an appropriate lower doping concentration [9, 15, 40].

The channel region of TFET is kept unintentionally doped in most TFET designs [8–10, 15]. Although simulations show that the lightly doped channel will not change the turn-on properties significantly [21], $I_{ON}$ increases simultaneously with increasing doping concentration of the channel [44]. The drain side doping significantly influences the performance of TFET devices especially at OFF-state due to the ambipolar characteristics as discussed in Section 2.5. As a result, an appropriate doping concentration in the drain region is also necessary to balance series resistance and ambipolar leakage.

The selection of band gap energies of source, channel, and drain is another key factor during the design of TFET structures. Using a smaller band gap material in the source is predicted to significantly enhance the tunneling current [36, 45]. However, the reduction of source material band gap also introduces the risk of increasing $I_{OFF}$ due to the enhanced thermal emission at OFF-state, which is proportional to $e^{-E_{a}}$. In practice, the channel material with a larger band gap is preferred to reduce the standby leakage current caused by thermal generation. The channel material with a larger band gap can also provide higher joint density of states to accept the source electrons. However, in the mixed As/Sb staggered gap n-type heterostructure TFET using GaAs$_{0.35}$Sb$_{0.65}$ as the source and In$_{0.7}$Ga$_{0.3}$As as the channel and drain, a channel material with higher Indium (In) composition (corresponds to lower In$_{0.7}$Ga$_{0.3}$As band gap) is needed to reduce $E_{a}$ and enhance $I_{ON}$. Given these material considerations, an appropriate channel band gap should be selected to yield reasonable large $I_{ON}$ without increasing excessive leakage [39]. The band gap of the drain side is usually selected to be large in order to introduce asymmetric to reduce the ambipolar leakage from drain to channel.

### 3.3 High-$\kappa$ gate dielectric

The gate dielectric determines the capacitive coupling of the gate with the tunnel junction in a TFET device [16]. It has already been reported that high-$\kappa$ gate dielectric provides the gate with better capacitive control of the tunnel junction [2, 10], which leads to better performance of TFET devices, both steeper SS and higher $I_{ON}$. As shown in Figure 12A, Boucart and Ionescu [3] demonstrated by simulation that $I_{ON}$ of TFETs increases as the gate dielectric constant increases. In Figure 12A, Si$_3$N$_4$ ($\varepsilon=7.5$) and two high-$\kappa$ gate dielectric with dielectric constants of 21 and 29 (such as HfO$_2$ and ZrO$_2$) are compared with SiO$_2$ ($\varepsilon=3.9$), all of which has a physical thickness of 3 nm. It can also be found in Figure 12A that, in addition to the improvement of $I_{ON}$, both the point SS and average SS are improved due to the better gate coupling given by a high-$\kappa$ dielectric [2, 3, 21]. Despite the high dielectric constant, the thickness of high-$\kappa$ gate dielectric also significantly influences the performance of TFETs. Mohata et al. [15] demonstrated that by scaling the electrical oxide thickness ($T_{OX}$) of gate dielectric (Al$_2$O$_3$/HfO$_2$ stack) from 2.3 nm to 2 nm, an enhancement of $I_{ON}$ by a factor of 3.5 was obtained in an n-channel GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As staggered gap TFET. However, the reduction of gate dielectric thickness also introduces the risk of increasing in gate leakage. Zhao et al. [10] reported in In$_{0.7}$Ga$_{0.3}$As TFETs that with 8 nm HfO$_2$ gate dielectric, both SRH G-R and BTBT currents contribute to $I_{OFF}$; however, for TFETs with 5 nm HfO$_2$ gate oxide, the gate leakage current also contributes to $I_{OFF}$, resulting in a smaller $E_{a}$ (activation energy). In addition to the improvement of ON-state performance, the high-$\kappa$ dielectric also provides the gate with better control of turning OFF the device, especially at a shorter gate length [16].

While high-$\kappa$ gate dielectrics have advantages for device performance, they can also bring in defects at the semiconductor/high-$\kappa$ interface if the high-$\kappa$ gate dielectric is deposited directly on the channel material [21], which will introduce the deleterious effects on the carrier mobility of the device [16, 21, 46, 47]. Although the drive current of TFETs is less sensitive to the changes of channel mobility than MOSFETs because the tunneling transport at the source/channel junction dominates any scattering in the channel, these interface defects will deteriorate the performance of TFETs and lead to degradation of SS. These interface traps can retard the Fermi level movement of the intrinsic channel layer, which is controlled by the gate bias, and they can also result in interface trap-assisted tunneling and subsequent thermal emission, which causes the high temperature dependence of SS [15, 23, 48, 49]. To reduce these interface states and also
to be compatible with standard complementary metal-oxide-semiconductor (CMOS) fabrication techniques, an interfacial oxide layer with a better oxide/semiconductor interface is required between the high-κ gate dielectric and the semiconductor channel. Zhao et al. [10] compared the performance of an In0.7Ga0.3As TFET with and without the interfacial oxide layer, which shows that Al2O3/HfO2 bilayer gate oxides effectively improve SS compared with single HfO2 gate oxide due to a better InGaAs/oxide interface. By contrast, Al2O3/HfO2 bilayer oxides do not show an effective improvement of \( I_{\text{on}} \) compared with single HfO2 gate oxide, which also proved that the \( I_{\text{on}} \) of TFETs primarily depends on the tunneling probability at the source/channel interface instead of channel electron mobility.

### 3.4 Channel length

The channel length of TFETs is not as critical as that of MOSFETs on determining the ON-state performance as the \( I_{\text{on}} \) of TFETs is determined by the tunneling current at the source/channel junction instead of scattering in the channel. By contrast, OFF-state leakage of TFETs is greatly dependent on channel length especially as the channel length is aggressively scaled. Figure 12B [16] shows the simulated transfer characteristics of TFETs using high-κ gate dielectric (\( \varepsilon = 25 \)) without the interfacial oxide layer with different gate lengths. It can be seen from Figure 12B, without a noticeable change of \( I_{\text{on}}/I_{\text{off}} \) increases by several orders of magnitude with scaling of channel length, especially as the channel length is less than 50 nm [16], which indicates that the gate lost its ability to efficiently turn off the device. This can be explained by the Zener breakdown mechanism [16, 50], where electrons can still tunnel through the tunnel junction at OFF-state without gate voltage. The reduced channel length decreases the tunneling barrier width from source to channel and results in Zener breakdown in TFET devices.

Baba [51] predicted that it would be possible to scale TFETs (surface tunnel transistors) to a gate length equal to the depletion layer width, on the order of 10 nm, where electron tunneling is suppressed. In an un gated p-i-n diode, the depletion region includes the entire intrinsic region in addition to the depleted areas of the p- and n-regions. Figure 13A and B [16] demonstrates the electron and hole concentrations of the cross-section of a TFET using different gate dielectrics (\( \varepsilon = 3.9 \) and \( \varepsilon = 25 \)), the high-κ gate dielectric is without the interfacial oxide layer) by simulations. With the scaling of channel length, the depleted regions are becoming narrower and less defined. At channel length of 10 nm, devices with both types of gate dielectrics are showing Zener breakdown (electron tunneling) at OFF-state.

Another way to check the depletion region width is to examine the energy band diagram across the TFET devices [16, 21]. The depletion region corresponds to the region between the flat band within the n-type region and the flat band within the p-type region in energy band diagrams. As shown in Figure 14A and B [16] for TFET band diagrams using different gate dielectrics (\( \varepsilon = 3.9 \) and \( \varepsilon = 25 \)), the high-κ gate dielectric is without the interfacial oxide layer.
layer) by simulations, both devices are effectively turned OFF with the well-defined depletion region with a channel length of 40 nm. When the channel length was reduced to 20 nm, the TFET using low gate dielectric ($\varepsilon = 3.9$) begins to break down. At a channel length of 10 nm, the devices break down in both cases with a tunneling barrier width less than 10 nm. In that case, neither of the devices can be well turned OFF, and the gate lost its control to the tunneling barrier modulation, resulting in high leakage current as shown in Figure 12B. As a result, the channel length of TFETs cannot be aggressively scaled to result in the Zener breakdown of the device.

**Figure 13**  Electron and hole concentrations of the cross-section of a TFET using different gate dielectrics, (A) $\varepsilon = 25$ and (B) $\varepsilon = 3.9$; there is no interfacial oxide layer within the high-$\kappa$ gate dielectric stacks. With the scaling of channel length, the depleted regions become narrower and less defined. With channel length=10 nm, devices with both types of gate dielectrics are showing Zener breakdown (electron tunneling) at OFF-state, although the high-$\kappa$ device shows a small advantage of showing a lower carrier concentration in the intrinsic region under the gate. Reprinted from Ref. [16], with permission, from Elsevier.

**Figure 14**  Schematic band diagrams of TFETs with different gate dielectrics, (A) $\varepsilon = 25$ and (B) $\varepsilon = 3.9$; there is no interfacial oxide layer within the high-$\kappa$ gate dielectric stacks. With a channel length of 40 nm, both devices are effectively turned off and the depletion region was well defined. When the channel length was reduced to 20 nm, the TFET using low gate dielectric ($\varepsilon = 3.9$) begins to break down. At channel length of 10 nm, the devices break down in both cases with a tunneling width less than 10 nm. Reprinted from Ref. [16], with permission, from Elsevier.
3.5 Comprehensive consideration of TFET design

On the basis of the discussions above, structure and device design optimization should be applied to increase $I_{on}$, reduce $I_{off}$, and improve SS, simultaneously, to offer a device with a comprehensive desirable performance. As the TFET is a device depending on the BTBT mechanism at the source/channel junction to transport carriers, the tunneling probability determines the tunneling current of a TFET device. To achieve higher tunneling probability, the tunneling barrier should be reduced, which can be achieved by using higher source doping concentration, smaller band gap source material, and staggered or broken band alignment. As high degeneration caused by heavily source doping will reduce available states for tunneling and thus degrade $I_{on}$ and SS [39], a modulated heavily pocket doping layer only near the tunnel junction is essential [15]. In addition, a direct band gap and smaller carrier effective mass can also contribute to improve $I_{on}$ [11–14]. In this respect, III–V materials are highly attractive, as they typically have low effective carrier mass and direct band gaps that allow for efficient tunneling [37].

Another optimization criterion is to reduce $I_{off}$, including all leakage current components: ambipolar leakage, SRH G-R leakage, and tunneling leakage. To reduce ambipolar current, asymmetric configuration, both asymmetric band gaps and asymmetric doping concentration between the source and drain should be introduced for the design of TFET structures [34]. Considering a source region with smaller band gap and higher doping is necessary to increase $I_{off}$, the drain material should be designed to have a relatively larger band gap and lower doping concentration (but not too low to increase serial resistance). Besides, to reduce SRH G-R leakage, large band gap materials are desired, but large band gap materials are not desired for ON-state performance. As a result, the material band gaps should be carefully selected to achieve higher $I_{on}$ without scarifying $I_{off}$. Furthermore, to reduce tunneling leakage, the tunnel barrier at the source/channel junction should be enlarged to block unwanted tunneling at OFF-state [13], which can be achieved by homojunction or staggered band alignment. As the homojunction TFET has its own drawback for low $I_{on}$, the staggered band alignment is a preferable choice for TFET design to achieve higher $I_{on}$ and lower $I_{off}$. Besides, the tunneling barrier height should also be well modulated for a staggered band alignment to achieve a balance between high $I_{on}$ and low $I_{off}$.

A sharp interface at the source/channel junction is needed to achieve steep SS, which requires both abrupt doping profile and minimum atom interdiffusion. To achieve better gate control to the channel energy bands movement, a high-$\kappa$ gate dielectric is also necessary. Besides, an interfacial oxide layer is needed between high-$\kappa$ gate dielectric and channel to reduce carrier scattering at the channel/oxide interface. In addition, it has been increasingly clear that the high-$\kappa$ dielectric on the Al bearing III-V compounds showed an increased SS due to larger interface induced defects ($D_\infty$) [52]. As a result, a channel material without Al components is also beneficial to achieve steeper SS.

All the above considerations related to TFET design are summarized in Figure 15. In view of all these considerations, mixed As/Sb based heterostructures, namely, GaAs$_{y}$Sb$_{1-y}$/In$_x$Ga$_{1-x}$As are very attractive as they allow a wide range of band gaps and staggered band alignments depending on the alloy compositions in the source and channel materials. Band alignments at the source/channel heterointerface can be tailor-made by carefully controlling the compositions of the mixed As/Sb material system while keeping this material system internally lattice matched. Besides, a sharp heterojunction interface and an abrupt doping profile can also be achieved by molecular beam epitaxy (MBE). Minimum atom interdiffusion can be realized by carefully controlling the shutter sequence during switching from Sb-rich material to As-rich material [11]. As a result, the mixed As/Sb staggered gap TFET is considered as a promising option for high-performance, low-standby power, and energy-efficient logic application. In the following section, we discuss the existing and state-of-the-art research aimed at the design, material growth, structure optimization, material characterization, device fabrication, together with their experimental or simulated structural properties and device performance.

4 Mixed As/Sb staggered gap TFETs

4.1 Composition and tunneling barrier height engineering

One of the key advantages of the GaAs$_{y}$Sb$_{1-y}$/In$_x$Ga$_{1-x}$As material system is that it can modulate the $E_{beff}$ easily and accurately by carefully controlling the alloy compositions in GaAs$_{y}$Sb$_{1-y}$ and In$_x$Ga$_{1-x}$As layers while keeping the material system to be internally lattice matched. Figure 16 shows the simulated changing trade (red dashed line) between $E_{beff}$ and In/Sb compositions. The inset demonstrated the band alignment of GaAs$_{y}$Sb$_{1-y}$/In$_x$Ga$_{1-x}$As without bias and the definition of $E_{beff}$ is also shown in
Figure 16. It can be seen from Figure 16 that $E_{\text{beff}}$ decreases linearly with increasing In and Sb compositions. This $E_{\text{beff}}$ plays a significant role in the performance of a TFET device, which not only determines the ON-state tunneling rate but also sets the blocking barrier for OFF-state leakage [9, 13]. Mohata et al. [9, 15] studied GaAs$_y$Sb$_{1-y}$/In$_x$Ga$_{1-x}$As n-type TFETs with different $E_{\text{beff}}$ by changing alloy compositions in source and channel materials. The schematic diagram of these TFET layer structures with different alloy compositions is shown in Figure 17A–C, respectively. These three structures were grown by solid source MBE on semi-insulating InP substrates. For the GaAs$_{0.5}$Sb$_{0.5}$/In$_{0.53}$Ga$_{0.47}$As structure, the active regions are lattice matched to the InP substrate; however, both the other two structures (GaAs$_{0.4}$Sb$_{0.6}$/In$_{0.65}$Ga$_{0.35}$As and GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As) are lattice mismatched to the InP substrate. To accommodate the lattice-mismatch-induced defects, linearly graded In$_x$Al$_{1-x}$As buffers were used in these two structures. Table 1 summarizes the structural information and device performance of these three structures. It can be seen from Table 1 that the $I_{\text{on}}$ of TFETs increases with scaling of $E_{\text{beff}}$. As a result, reducing $E_{\text{beff}}$ is one efficient way to boost the ON-state performance of TFETs. However, the scaling of $E_{\text{beff}}$ also introduces the risk of increasing $I_{\text{off}}$. Firstly, both direct BTBT and trap-assisted tunneling (TAT) leakage are enhanced due to reduced tunneling barrier height. Secondly, band gap energies of both GaAs$_y$Sb$_{1-y}$ and In$_x$Ga$_{1-x}$As are decreasing with increasing Sb and In compositions, which will increase SRH G-R leakage current. Besides, the increased Sb composition in the GaAs$_y$Sb$_{1-y}$ layer also brings in the potential of atom interdiffusion at the heterointerface. As
a result, proper interfacing engineering at the GaAs \textsubscript{y}Sb \textsubscript{1-y} /In \textsubscript{x}Ga \textsubscript{1-x}As heterointerface is indispensable to achieve superior structural properties and device performance, which will be discussed in detail in the next section.

4.2 Interfacing engineering

Engineering an abrupt source/channel heterointerface is needed for type II staggered gap TFETs. However, the abrupt switching from mixed anion GaAs \textsubscript{y}Sb \textsubscript{1-y} to mixed cation In \textsubscript{x}Ga \textsubscript{1-x}As is a significant growth challenge due to different surface sticking coefficients of As and Sb at the specific growth temperature \cite{13}. Furthermore, improper change of group V fluxes at the source and channel interface will introduce intermixing between As and Sb that leads to uncontrolled layer composition at the heterointerface, which in turn produces high dislocation density in this region \cite{11,13}. These dislocations will introduce fixed charges \cite{53} at the source/channel interface and thus it will affect the band alignment as well as the value of \( E_{\text{eff}} \). In practice, high Sb and In composition is used in GaAs \textsubscript{y}Sb \textsubscript{1-y} and In \textsubscript{x}Ga \textsubscript{1-x}As layers, respectively, to reduce \( E_{\text{eff}} \) and improve \( I_{\text{ON}} \). The high Sb composition further increased the growth challenge for engineering an abrupt heterointerface with superior quality. When it comes to the specific layer structure as shown in Figure 17C, two different surface terminations, i.e., (i) GaAs-like and (ii) InAs-like can be realized when switching from Sb-rich GaAs \textsubscript{0.35}Sb \textsubscript{0.65} and to As-rich In \textsubscript{0.7}Ga \textsubscript{0.3}As. For the former case, the GaAs-like interface was formed by the residual Ga atoms in the growth chamber together with As over-pressure. For the latter case, 1–2 monolayers (MLs) of In were added intentionally prior to the growth of In \textsubscript{x}Ga \textsubscript{1-x}As layer when the As flux was ramping up from 35% to 100% \cite{9,11}. If the GaAs-like interface formed at the GaAs \textsubscript{0.35}Sb \textsubscript{0.65} /In \textsubscript{0.7}Ga \textsubscript{0.3}As heterointerface, the lattice mismatch between the top In \textsubscript{0.7}Ga \textsubscript{0.3}As layer and the GaAs-like interface is as large as 5%, which gives high possibility to generate dislocations at the interface and inside the In \textsubscript{0.7}Ga \textsubscript{0.3}As top layer. By contrast, if the InAs-like interface formed, this mismatch is only limited to 2%, which provides a better basis for the growth of the top In \textsubscript{0.7}Ga \textsubscript{0.3}As layer. These two different interface engineering types will influence both the structural properties and the device performance of the mixed As/Sb staggered gap TFETs, which will be discussed separately in detail in the following sections.

![Figure 17](image)

**Figure 17** Schematic layer diagram of GaAs \textsubscript{y}Sb \textsubscript{1-y} /In \textsubscript{x}Ga \textsubscript{1-x}As staggered gap TFET structures with different alloy compositions. (A) GaAs \textsubscript{0.5}Sb \textsubscript{0.5} /In \textsubscript{0.53}Ga \textsubscript{0.47}As structure shows an \( E_{\text{eff}} \) of 0.5 eV; (B) GaAs \textsubscript{0.4}Sb \textsubscript{0.6} /In \textsubscript{0.65}Ga \textsubscript{0.35}As structure shows an \( E_{\text{eff}} \) of 0.31 eV; (C) GaAs \textsubscript{0.35}Sb \textsubscript{0.65} /In \textsubscript{0.7}Ga \textsubscript{0.3}As structure shows an \( E_{\text{eff}} \) of 0.25 eV. All \( E_{\text{eff}} \) values are from simulation. Reprinted from Ref. \cite{9} and Ref. \cite{15}, with permission, from IEEE.

### Table 1

<table>
<thead>
<tr>
<th>Source</th>
<th>Channel</th>
<th>Drain</th>
<th>( E_{\text{eff}} ) eV</th>
<th>( I_{\text{ON}} ) ( \mu \text{A}/\mu\text{m} )</th>
</tr>
</thead>
<tbody>
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<td>(a) \textsuperscript{p++-GaAs}<em>{0.5}Sb</em>{0.5}</td>
<td>i-In \textsubscript{0.55}Ga \textsubscript{0.45}As</td>
<td>n-In \textsubscript{0.53}Ga \textsubscript{0.47}As</td>
<td>0.5</td>
<td>60</td>
</tr>
<tr>
<td>(b) \textsuperscript{p++-GaAs}<em>{0.55}Sb</em>{0.45}</td>
<td>i-In \textsubscript{0.65}Ga \textsubscript{0.35}As</td>
<td>n-In \textsubscript{0.63}Ga \textsubscript{0.37}As</td>
<td>0.31</td>
<td>78</td>
</tr>
<tr>
<td>(c) \textsuperscript{p++-GaAs}<em>{0.35}Sb</em>{0.65}</td>
<td>i-In \textsubscript{0.8}Ga \textsubscript{0.2}As</td>
<td>n-In \textsubscript{0.8}Ga \textsubscript{0.2}As</td>
<td>0.25</td>
<td>135</td>
</tr>
</tbody>
</table>
4.3 Structural properties of mixed As/Sb staggered gap TFETs with different interface engineering

Different terminated interface atoms determine the lattice-mismatch between the top layer and the interface layer [11], and different interface engineering can also introduce different amounts of fixed positive charges [11, 13], both of which will influence the structural properties of these structures, including strain relaxation properties, surface morphologies, and dislocation densities.

4.3.1 Strain relaxation properties

The strain relaxation properties of epilayers can be characterized using X-ray diffraction. Out-of-plane lattice constant and in-plane lattice constant can be obtained from reciprocal space maps (RSMs) using symmetric scan and asymmetric scan, respectively. The relaxation states and residual strain of each epilayer can be calculated from the obtained lattice constants. The symmetry of the relaxation states of each epilayer can also be compared by aligning the incident X-ray beam along different directions. For the TFET structure as shown in Figure 17C, the symmetric (004) and asymmetric (115) RSMs of the InAs-like interface structure are shown in Figure 18A and B, respectively, with incident X-ray beam along the [1ī0] direction. Each layer was labeled to its corresponding reciprocal lattice point (RLP) based on wet chemical etching experiments [11]. As shown in Figure 18A and B, four distinct RLP maxima were found in RSMs of InAs-like interface structure, corresponding to (i) the InP substrate, (ii) GaAs$_{0.35}$Sb$_{0.65}$ source layer, (iii) In$_{0.7}$Ga$_{0.3}$As channel/drain layer, and (iv) the 100 nm In$_{0.3}$Al$_{0.7}$As uppermost layer of the linearly graded In$_{0.7}$Al$_{0.3}$As buffer. Owing to the residual strain within the GaAs$_{0.35}$Sb$_{0.65}$, In$_{0.7}$Ga$_{0.3}$As, and In$_{0.3}$Al$_{0.7}$As buffer layers together with heavily C doping caused lattice contraction in the GaAs$_{0.35}$Sb$_{0.65}$ layer; these three layers with the same designed lattice constant were shown in separate RLPs. Detailed strain relaxation analysis based on the symmetric (004) and asymmetric (115) RSMs show symmetric strain relaxation states of the InAs-like structure along [1ī0] and [1ī0] directions (the symmetric and asymmetric RSMs of the InAs-like interface structure with incident X-ray beam along the [1ī0] direction are not shown in this review but can be found in Ref. [11]). Only ~4% strain relaxation in In$_{0.7}$Ga$_{0.3}$As and GaAs$_{0.35}$Sb$_{0.65}$ active layers with respect to the In$_{0.3}$Al$_{0.7}$As “virtual substrate” was obtained from the InAs-like interface structure [11], suggesting the pseudomorphic nature of these two layers, indicating that few dislocations formed within the active region of this structure.

Similarly, the symmetric (004) and asymmetric (115) RSMs of the GaAs-like interface structure are shown in Figure 19A and B, respectively, with incident X-ray beam along the [1ī0] direction. Different from the RSMs of the InAs-like interface structure, one can see from Figure 19A and B that the contour of the In$_{0.3}$Ga$_{0.7}$As channel/drain layer was merged with the GaAs$_{0.35}$Sb$_{0.65}$ source layer in RSMs of the GaAs-like interface structure. A higher percentage of strain relaxation of 94% of these two layers with respect to InP substrate than that in the InAs-like interface structure [11], suggesting the pseudomorphic nature of these two layers, indicating that few dislocations formed within the active region of this structure.

![Figure 18](image1.png)  
(A) Symmetric (004) and (B) asymmetric (115) RSMs of the InAs-like interface TFET with a layer structure as shown in Figure 17C using an incident X-ray beam along the [1ī0] direction. Reprinted from Ref. [11], with permission, from the American Institute of Physics, copyright (2012), AIP Publishing LLC.

![Figure 19](image2.png)
interface structure, which is \( \sim 75\% \) for the In\(_{0.7}\)Ga\(_{0.3}\)As layer and \( \sim 80\% \) for the GaAs\(_{0.35}\)Sb\(_{0.65}\) layer, respectively \([11]\) was calculated. A higher degree of strain relaxation states indicates higher dislocation density within these two layers, supported by larger elongation of the corresponding RLP along the \( x \)-axis of the RSM. In fact, the elongation of this RLP is highly enfeebled after removing the top In\(_{0.7}\)Ga\(_{0.3}\)As layer from the GaAs-like interface structure, and the relaxation value of the GaAs\(_{0.35}\)Sb\(_{0.65}\) layer of the GaAs-like interface structure was recalculated and found to be \( \sim 80\% \) after etching the top In\(_{0.7}\)Ga\(_{0.3}\)As layer, which is fairly identical with that in the GaAs-like interface structure \([11]\). The above results reveal that the GaAs\(_{0.35}\)Sb\(_{0.65}\) layer is not as defective as the In\(_{0.7}\)Ga\(_{0.3}\)As layer in the GaAs-like interface structure and the higher dislocation density is only confined within the top In\(_{0.7}\)Ga\(_{0.3}\)As layer.

The lattice parameters, mismatch, composition, and relaxation of each layer from both the InAs-like interface and GaAs-like interface structures are summarized in Table 2 \([11]\). As shown in Table 2, both of these structures show symmetric strain relaxation along two orthogonal \([110]\) and \([\bar{1}10]\) directions, indicating approximately equal amount of \( \alpha \) and \( \beta \) dislocations formed in the relaxation of strain. In addition, from the measured in-plane and out-of-plane lattice constants of the InAs-like interface structure, the pseudomorphic nature of GaAs\(_{0.35}\)Sb\(_{0.65}\)/In\(_{0.7}\)Ga\(_{0.3}\)As was confirmed, indicating low dislocation within these two layers. Therefore, the InAs-like interface TFET structure creates a “virtually” defect-free active region than the GaAs-like interface TFET structure, which is desirable for improving the performance of TFET devices with lower OFF-state \( p^\cdot i^\cdot n^+\) leakage and higher \( I_{\text{ON}}/I_{\text{OFF}} \) ratio.

### 4.3.2 Surface morphology

The study of surface morphology of metamorphic structures is an important figure of merit due to the expected crosshatch pattern resulting from ideal strain relaxation with minimum concentrations of threading dislocations. For the TFET structure as shown in Figure 17C, surface morphology of the TFET structures with different source/channel interface engineering was examined by atomic force microscopy (AFM) in contact mode from the top In\(_{0.7}\)Ga\(_{0.3}\)As surface. The 20 \( \mu \)m \( \times \) 20 \( \mu \)m AFM micrographs of the InAs-like interface structure and GaAs-like interface structure and related line profiles in two orthogonal \(<110>\) directions are shown in Figures 20 and 21, respectively. From Figure 20, the anticipated two-dimensional crosshatch pattern is well developed and fairly uniform, as expected for an ideal graded buffer, from the InAs-like interface TFET structure. The peak-to-valley height from line profiles in the two orthogonal \(<110>\) direction is also included in these figures. The uniform distribution of the crosshatch pattern from \([110]\) and \([\bar{1}10]\) directions for the InAs-like interface TFET structure suggests a symmetric relaxation of the linearly graded buffer layer, which is in agreement with X-ray diffraction (XRD) results. The AFM micrograph of the InAs-like interface structure shows a smooth surface morphology with surface root-mean-square (\( \text{rms} \)) roughness of 3.17 nm. Compared with the surface morphology of the InAs-like interface, the GaAs-like interface structure does not exhibit two-dimensional crosshatch surface morphology. A grainy texture dispersed crossing the surface was observed from...
Table 2 Summary of the InAs-like interface and GaAs-like interface TEFT structures with incident X-ray beam along [110] and [110] directions.a

<table>
<thead>
<tr>
<th>Sample</th>
<th>Incident beam direction</th>
<th>Layers</th>
<th>Lattice constant, Å</th>
<th>Composition</th>
<th>Relaxation, %</th>
<th>Tilt, as</th>
<th>Strain, %</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) GaAs-like interface</td>
<td>[110]</td>
<td>InGaAs/GaAsSb</td>
<td>c = 5.9401, a = 5.9322, a_r = 5.9361</td>
<td>In: 70% Sb: 65%</td>
<td>94</td>
<td>-37</td>
<td>1.15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>InAlAs</td>
<td></td>
<td></td>
<td>73</td>
<td>-43</td>
<td>1.14</td>
</tr>
<tr>
<td></td>
<td>[110]</td>
<td>InGaAs/GaAsSb</td>
<td>c = 5.9400, a = 5.9284, a_r = 5.9342</td>
<td>In: 69% Sb: 64%</td>
<td>91</td>
<td>-145</td>
<td>1.11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>InAlAs</td>
<td></td>
<td></td>
<td>74</td>
<td>-164</td>
<td>1.15</td>
</tr>
<tr>
<td>(b) InAs-like interface</td>
<td>[110]</td>
<td>GaAsSb</td>
<td>c = 5.9249, a = 5.9064, a_r = 5.9157</td>
<td>Sb: 64%</td>
<td>80</td>
<td>-19</td>
<td>0.80</td>
</tr>
<tr>
<td></td>
<td></td>
<td>InGaAs</td>
<td></td>
<td></td>
<td>75</td>
<td>-43</td>
<td>1.08</td>
</tr>
<tr>
<td></td>
<td></td>
<td>InAlAs</td>
<td></td>
<td></td>
<td>72</td>
<td>-44</td>
<td>1.29</td>
</tr>
<tr>
<td></td>
<td>[110]</td>
<td>GaAsSb</td>
<td>c = 5.9247, a = 5.9065, a_r = 5.9156</td>
<td>Sb: 64%</td>
<td>81</td>
<td>95</td>
<td>0.80</td>
</tr>
<tr>
<td></td>
<td></td>
<td>InGaAs</td>
<td></td>
<td></td>
<td>76</td>
<td>78</td>
<td>1.08</td>
</tr>
<tr>
<td></td>
<td></td>
<td>InAlAs</td>
<td></td>
<td></td>
<td>72</td>
<td>95</td>
<td>1.29</td>
</tr>
</tbody>
</table>

a c is out-of-plane lattice constant, a is in-plane lattice constant, and a_r is relaxed lattice constant. From Ref. [11].

the AFM micrograph of the GaAs-like interface structure. From the line profiles along [110] and [110] directions, the peak-to-valley height of the GaAs-like interface sample is three times higher than the InAs-like interface structure, indicating significantly poor surface quality due to the large amount of dislocation embedded within the TFET structure. The surface rms roughness of the GaAs-like interface sample is 4.46 nm, which is much higher than that of the InAs-like interface structure. The rough surface and deterioration of the two-dimensional crosshatch pattern on the surface of the GaAs-like interface structure should be attributed to the higher dislocation density of the InGaAs layer introduced by the GaAs-like interface, which was also confirmed by broadening of the RLP during X-ray measurement as introduced in Section 4.3.1. From the AFM micrographs of these two structures, it can be concluded that the InAs-like interface structure shows a much better surface morphology with typical two-dimensional crosshatch patterns and lower peak-to-valley height corresponding to a reduced rms roughness compared with the GaAs-like interface structure. As the two structures are identical except the interface between InGaAs and GaAsSb, one can expect a much lower defect density in the InAs-like interface TFET structure and superior electrical transport properties [11].

4.3.3 Dislocation and defects

To further investigate the influence of different terminated atoms to the structural properties of mixed As/Sb staggered gap TFET structures, the dislocations, defects, and the crystalline quality of both GaAs-like interface and InAs-like interface structures are characterized by cross-sectional transmission electron microscopy (TEM) analysis. Figure 22A and B show cross-sectional TEM micrographs of InAs-like interface and GaAs-like interface structures, respectively. All layers were labeled in Figure 22A, B and the GaAs/Sb/InGaAs interface was denoted by an arrow in each micrograph. One can see from Figure 22A, B that the linearly graded InAlAs buffer layer effectively accommodates the lattice mismatch-induced dislocations between the active layers and the InP substrate in both structures. No threading dislocations were observed in the GaAs/Sb layers grown on the linearly graded InAlAs buffers in both structures, indicating that the InAlAs buffer effectively accommodates the lattice mismatch between the active layer and the InP substrate and thus provides a high-quality virtual substrate for TFET structures.

It can be seen from Figure 22A that no threading dislocations were observed in the top InGaAs layer of the InAs-like interface TFET structure at this magnification, indicating a threading dislocation density (TDD) in this layer on the order of or below $\sim 10^7$/cm$^2$. The low dislocation density of the InGaAs layer in the InAs-like interface structure leads to a superior surface and well-developed two-dimensional crosshatch pattern from the linearly graded buffer, both of which are confirmed with the results from AFM analysis. Moreover, the low dislocation density also contributes to the pseudomorphic characteristic of the InGaAs layer and the small $\Delta$ broadening of the RLP in RSMs from the InAs-like interface TFET structure. By contrast, high dislocation density
was detected in the In$_{0.7}$Ga$_{0.3}$As layer of the GaAs-like interface TFET structure. Threading dislocations were generated from the interface of GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As and went all the way up through the In$_{0.7}$Ga$_{0.3}$As layer. The dislocation density in the In$_{0.7}$Ga$_{0.3}$As layer was too high to be quantified. As no dislocation was observed from the bottom GaAs$_{0.35}$Sb$_{0.65}$ layer on which the In$_{0.7}$Ga$_{0.3}$As was grown, it was reasonable to conclude that the GaAs-like interface contributed to the high dislocation density in the In$_{0.7}$Ga$_{0.3}$As layer and it is consistent with the XRD analysis discussed in Section 4.3.1. Moreover, it is also clear that the poor surface morphology of the GaAs-like interface TFET structure from AFM measurement and the
elongation of the RLP in RSMs are due to a very high defect density present in the top In$_{0.7}$Ga$_{0.3}$As layer, as observed by cross-sectional TEM.

On the basis of the above analysis, the InAs-like interface provides a high-quality TFET structure compared with the GaAs-like interface, where higher dislocations are detected in the channel and drain In$_{0.7}$Ga$_{0.3}$As layer, as characterized from X-ray, AFM, and cross-sectional TEM analysis. The higher dislocation density at the source/channel interface and within the channel/drain layer of the GaAs-like interface structure will enhance both the SRH G-R and tunneling process at the heterointerface, which will contribute to the higher OFF-state leakage current and degrades the $I_{ON}/I_{OFF}$ ratio of the TFET devices.

### 4.4 Device fabrication

A main challenge for the fabrication of MBE grown vertical heterostructure TFETs is to perfectly align the gate on the channel area. There are several different TFET device structures reported in the literature based on different fabrication processes, such as single vertical side wall device structure [8, 23, 54], ring-type vertical side wall device structure [10, 55], self-aligned gate nanopillar device structure [9, 15, 56, 57], etc. To further increase $I_{on}/I_{off}$ double gate [16] or gate-all-round TFET [10, 56] device designs are used. Besides, the device design demands extremely scaled gate oxide EOT and ultra-thin body geometry in order to achieve low $I_{off}$ and desired transistor performance [56]. Mohata et al. [56] proposed a vertical TFET fabrication process with a self-aligned gate, which can ultimately lead to the ultra-thin gate-all-round device geometry to achieve superior TFET performance.

Figure 23 shows the cross-section schematics of the fabricated TFET device following by key process steps, reported in Ref. [56]. A summary of the entire fabrication process flow is also shown in Figure 23. For the layer structures as shown in Figure 17C, 250 nm thick molybdenum (Mo) was blanket-deposited on the n$^+$ In$_{0.7}$Ga$_{0.3}$As layer, as characterized from X-ray, AFM, and cross-sectional TEM analysis. The higher dislocation density at the source/channel interface and within the channel/drain layer of the GaAs-like interface structure will enhance both the SRH G-R and tunneling process at the heterointerface, which will contribute to the higher OFF-state leakage current and degrades the $I_{ON}/I_{OFF}$ ratio of the TFET devices.
is shown in Figure 24A, and the corresponding tilted view scanning electron microscopy (SEM) micrograph is shown in Figure 24B [11], respectively. Figure 24C [56] shows the cross-sectional TEM image of the fabricated TFET device with a 250-nm drawn mesa width.

4.5 OFF-state performance

As shown in Section 4.3, different terminated atoms at the GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As heterointerface greatly influence structural properties of TFET structures. These differences in structural properties, such as strain relaxation and defect density differences, will further influence device performance. Especially, the high dislocation density at the source/channel interface of the GaAs-like interface structure may change the OFF-state transport mechanism of the fabricated devices and lead to high leakage current. To assess the impact of different interface engineering on the OFF-state performance of TFETs, two sets of p$^+$-i-n$^+$ diodes were fabricated. As the OFF-state current of TFETs is governed by leakage current of the reverse-biased p$^+$-i-n$^+$ diode [11, 23], current-voltage (I-V) characteristics of these p$^+$-i-n$^+$ diodes were measured and compared. Figure 25 [11] shows the room temperature I-V characteristics of the p$^+$-i-n$^+$ diodes from the InAs-like interface and GaAs-like interface structure. Approximately four orders higher leakage current density was observed from the GaAs-like interface structure than the InAs-like interface p$^+$-i-n$^+$ diodes at 300 K, indicating that different OFF-state transport mechanisms are involved in these TFET structures. To gain insight into the OFF-state current mechanism for these TFET structures, temperature-dependent I-V measurements were carried out on these reverse-biased p$^+$-i-n$^+$ diodes with temperatures ranging from 150 K to 300 K, and simulations have been performed with Sentaurus [58] to explain the difference in OFF-state transport between two structures.

Figure 26A [11] shows the I-V characteristics of the reverse-biased p$^+$-i-n$^+$ diode at different measurement temperatures from the InAs-like interface device. One can see from Figure 26A that OFF-state leakage current increases exponentially with rising temperature. A field-enhanced SRH G-R model [59] was used to explain the OFF-state leakage mechanism of the InAs-like interface p$^+$-i-n$^+$ diode at different temperatures. A lower positive fixed charge density, $Q_f = 10^{12}$ cm$^2$, due to lower defect density at the source/channel interface was also incorporated in the simulation along with the field-enhanced SRH G-R process to explain OFF-state leakage current. The simulated I-V characteristics (Figure 26A, solid lines) are in good agreement with the measured data (Figure 26A, scattered line) at different temperatures, suggesting the validation of the model used in the InAs-like interface p$^+$-i-n$^+$ diode. Figure 26B [11] shows the Arrhenius plot of OFF-state leakage from the reverse-biased p$^+$-i-n$^+$ diode as a function of $1/kT$ at various reverse-bias voltages. A straight line fitting to these data points at a given reverse bias yield a gradient which corresponds to the activation energy of $E_a = E_s - E_r$, which is responsible for OFF-state leakage.
current generation. Here, $E_c$ stands for the conduction band minimum of channel near the source/channel interface and $E_T$ is the energy of trap states. One can see from Figure 26B that $E_c$ decreases with increasing reverse-bias voltage from 0.17 eV to 0.125 eV, resulting in an increasing leakage current trend. This is due to the fact that the electrical field intensity across the p'-i-n' diode was enlarged as increasing the reverse-bias voltage. The enlarged electrical field further increases band-bending, which leads to a stronger field-enhanced SRH G-R process across the interface.

Figure 27 [11] shows the I-V characteristics of the reverse-biased p'-i-n' diode at different measurement temperatures of the GaAs-like interface device. One can see from Figure 27 that OFF-state leakage current is much higher than that of the InAs-like interface device at each temperature step. Leakage current reduces with decreasing temperature from 300 K to 150 K, as expected, but the decreasing trend is not as strong as the InAs-like interface device. Moreover, the weaker temperature dependence and higher leakage current confirmed that the tunneling process dominates the OFF-state transport of the GaAs-like interface p'-i-n' diode, which is indeed the case due to higher dislocation density present in In$_{0.7}$Ga$_{0.3}$As channel and drain regions. A direct BTBT model [44] was performed to explain the observed high OFF-state current caused by high dislocation density observed at the GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As heterointerface. As shown in Figure 27 [11], the simulated I-V characteristics (solid lines) are in good agreement with the measured data (scattered lines) at all temperatures. To explain why the BTBT process dominates the OFF-state transport of the GaAs-like interface TFET structure, positive fixed charges caused by Tamm states and point defects, which are widely observed at the heterointerface of mixed As/Sb material systems [60, 61], were introduced at the GaAs-like interface region in the simulation. The fixed positive charges cause energy band bending at the GaAs-like heterointerface region. Figure 28A [11] shows the simulated band diagram of the GaAs-like interface TFET structure and the inset shows the position of the fixed positive charges in this energy.
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Charge density caused by Tamm states and point defects related to the high defect density at the GaAs-like interface leads to interband tunneling which dominates the OFF-state transport of the GaAs-like interface TFET structure.

By contrast, a lower positive fixed charge density, \( Q_f = 10^{12} \text{ cm}^{-2} \), due to lower defect density at the source/channel interface was incorporated in the simulation of OFF-state performance of the InAs-like interface device.

Figure 26  (A) Measured and simulated I-V characteristics of reverse-biased InAs-like interface GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As p'-i-n' diode for temperatures ranging from 150 K to 300 K and (B) an extraction of the activation energy for leakage current generation as a function of reverse bias voltage of InAs-like interface GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As p'-i-n' diode. The field-enhanced SRH G-R model is in good agreement with measured data. Activation energy shows dependence of reverse bias voltage. Reprinted from Ref. [11], with permission, from the American Institute of Physics, copyright (2012), AIP Publishing LLC.

Figure 27  Measured and simulated I-V characteristics of reverse-biased GaAs-like interface GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As p'-i-n' diode for temperatures ranging from 150 K to 300 K. The direct BTBT model is in good agreement with measured data at different temperature ranges. The small temperature dependence and the high leakage current confirm that the tunneling process is the dominating OFF-state transport mechanism in this structure. Reprinted from Ref. [11], with permission, from the American Institute of Physics, copyright (2012), AIP Publishing LLC.

Band diagram. A high fixed positive charge density of \( 1.5 \times 10^{13} \text{ cm}^{-2} \) due to higher defect density is needed to induce the large band bending in the GaAs-like interface structure to generate the OFF-state current as measured in different temperature steps. As shown in Figure 28A [11], the fixed charge density at this level can convert the band alignment of the TFET structure from staggered gap to broken gap, resulting in an overlap of the valence band of the GaAs_{0.35}Sb_{0.65} source with the conduction band of the In_{0.7}Ga_{0.3}As channel, causing the device to be normally ON even at OFF-state. As a result, the high fixed positive charge density caused by Tamm states and point defects related to the high defect density at the GaAs-like interface leads to interband tunneling which dominates the OFF-state transport of the GaAs-like interface TFET structure.

By contrast, a lower positive fixed charge density, \( Q_f = 10^{12} \text{ cm}^{-2} \), due to lower defect density at the source/channel interface was incorporated in the simulation of OFF-state performance of the InAs-like interface device. The simulated energy band diagram of the InAs-like interface TFET structure with a fixed interface charge density of \( Q_f = 10^{12} \text{ cm}^{-2} \) is shown in Figure 28B [11]. One can see from Figure 28B that the type-II staggered band alignment was well maintained in the InAs-like interface TFET structure, which leads to lower leakage current at OFF-state. The field-enhanced SRH G-R mechanism [59] is also observed in Figure 28B, where the carriers in the p' source region firstly tunnel into mid-gap states and a subsequent thermal emission process inject them into the conduction band of the channel. To gain further insight into the band alignment of these TFET structures as a function of fixed positive charge density within the source/channel interface region, simulation was performed to generate band diagrams at different \( Q_f \) values. As shown in Figure 29 [11], \( E_{\text{eff}} \) decreases with increasing value of \( Q_f \). One can see from Figure 28B that by varying the \( Q_f \) value, the band line-up can be converted from staggered to broken gap. Although a broken line-up yields the best ON-state performance, it can also increase...
can be achieved by minimizing the interface defect density in a TFET structure. The InAs-like interface provides lower defect density which leads to lower $Q_f$ at the source/channel heterointerface, resulting in well-maintained type-II staggered gap band alignment. It also leads to lower OFF-state leakage current, higher $I_{on}/I_{off}$ ratio, and shows great potential for future high-performance heterostructure TFETs for low-power logic applications.

### 4.6 Experimental determination of band alignments

During MBE growth of mixed As/Sb heterostructure TFETs, improper change of group-V fluxes at the source and channel interface will introduce intermixing between As and Sb atoms that leads to uncontrolled layer composition at this heterointerface, which in turn will produce high dislocation density in this region [9, 57]. These dislocations will introduce fixed charges at the source/channel interface [53] and thus it will affect band alignment as well as the value of $E_{\text{beff}}$ [11]. In Section 4.5, simulations showed that band alignment is converted from staggered gap to broken gap with a fixed positive charge density of $\sim 6 \times 10^{12}/\text{cm}^2$, corresponding to an $E_{\text{beff}}$ value of 0 eV. To maintain staggered band alignment, a lower $Q_f$ is indispensable, which

### Figure 29

Simulated band diagrams of GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As n-channel heterostructure TFET structures with different fixed charges at the source/channel interface region. The inset shows that the effective tunneling barrier height changes as a function of fixed charge density. Band alignment is converted from staggered gap to broken gap at the fixed charge density of $\sim 6 \times 10^{12}/\text{cm}^2$. Reprinted from Ref. [11], with permission, from the American Institute of Physics, copyright (2012), AIP Publishing LLC.
Therefore, it is necessary to verify this defect-assisted band alignment transition by experimental proof in a mixed As/Sb TFET heterostructure.

Kraut et al. [62] demonstrated one experimental method to determine the band offset of heterostructures by measuring the core level (CL) and valence band maxima (VBM) binding energies of the materials in the structure using X-ray photoelectron spectroscopy (XPS). To measure the valence band offset (VBO) of the GaAs<sub>y</sub>Sb<sub>1-y</sub>/In<sub>x</sub>Ga<sub>1-x</sub>As heterojunction, Sb<sub>3d<sub>5/2</sub></sub>/In<sub>3d<sub>5/2</sub></sub> CLs, and VBM of GaAs<sub>y</sub>Sb<sub>1-y</sub>/In<sub>x</sub>Ga<sub>1-x</sub>As should be detected. Zhu et al. [13, 14] measured the band alignments of the GaAs<sub>y</sub>Sb<sub>1-y</sub>/In<sub>x</sub>Ga<sub>1-x</sub>As heterojunction from three structures with different material composition and interface engineering, as discussed above. Structure A has a layer structure as shown in Figure 17B (GaAs<sub>0.4</sub>Sb<sub>0.6</sub>/In<sub>0.65</sub>Ga<sub>0.35</sub>As) with an InAs-like heterointerface; structure B has a layer structure as shown in Figure 17C (GaAs<sub>0.35</sub>Sb<sub>0.65</sub>/In<sub>0.7</sub>Ga<sub>0.3</sub>As) with an InAs-like heterointerface; structure C also has a layer structure as shown in Figure 17C (GaAs<sub>0.35</sub>Sb<sub>0.65</sub>/In<sub>0.7</sub>Ga<sub>0.3</sub>As) but with a GaAs-like heterointerface. The structural properties of structures B and C have already been discussed in Section 4.3. The structural properties of TFET structure A show similar properties as structure B due to the InAs-like interface within both of these structures. As a result, low dislocation density should be expected at the heterointerface of both structures A and B, but high dislocation density is expected at the heterointerface of structure C. Detailed XRD and cross-sectional TEM studies [13] also confirmed this speculation. Table 3 summarizes the composition, interface engineering, and defect density difference of these three TFET structures. As shown in Figure 30 [13], XPS spectra were collected from three samples of each structure: (i) 5 nm InGaAs/310 nm GaAsSb was used to measure CL binding energy of In and Sb at the interface; (ii) 150 nm InGaAs/310 nm GaAsSb was used to measure the CL binding energy of In and VBM of InGaAs; (iii) 310 nm GaAsSb without the top InGaAs layer was used to measure the CL binding energy of Sb and VBM of GaAsSb. XPS measurements were performed on a Phi Quantera Scanning XPS Microprobe instrument using a monochromatic Al Kα (1486.7 eV) X-ray source. In3d<sub>5/2</sub>, Sb3d<sub>5/2</sub>, CL, In<sub>x</sub>Ga<sub>1-x</sub>As valence (VB) and GaAs<sub>y</sub>Sb<sub>1-y</sub> VB spectra were recorded using pass energy of 26 eV. An exit angle of 45° was used in all measurements. Oxide layers on all sample surfaces were carefully removed by wet chemical etching using citric acid/hydrogen peroxide (C<sub>6</sub>H<sub>8</sub>O<sub>7</sub>:H<sub>2</sub>O<sub>2</sub>) at volume ratio of 50:1 for 10 s on the In<sub>x</sub>Ga<sub>1-x</sub>As surface and 1 min on the GaAs<sub>y</sub>Sb<sub>1-y</sub> surface, respectively, before loading into the XPS chamber. Approximately 2–3 nm was etched from each sample surface according to the premeasured etching rate [11].

Once the binding energy information from each sample surface was collected, the VBO can be determined by the Kraut [62] method:

\[
\Delta E_v = E_{GaAs_{y}Sb_{1-y}}^{VBM} - E_{GaAs_{y}Sb_{1-y}}^{CL} - E_{In_{x}Ga_{1-x}As}^{VBM} - E_{In_{x}Ga_{1-x}As}^{CL},
\]

\[\Delta E_{v}(i)\] (15)

Table 3 Summary of composition and defect density difference of TFET structures studied [13].

<table>
<thead>
<tr>
<th>Structure details</th>
<th>Composition</th>
<th>Channel/drain interface engineering</th>
<th>Defect density at the source/channel interface and in InGaAs layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>GaAs&lt;sub&gt;0.4&lt;/sub&gt;Sb&lt;sub&gt;0.6&lt;/sub&gt;</td>
<td>In&lt;sub&gt;0.65&lt;/sub&gt;Ga&lt;sub&gt;0.35&lt;/sub&gt;As</td>
<td>InAs-like Low</td>
</tr>
<tr>
<td>B</td>
<td>GaAs&lt;sub&gt;0.35&lt;/sub&gt;Sb&lt;sub&gt;0.65&lt;/sub&gt;</td>
<td>In&lt;sub&gt;0.7&lt;/sub&gt;Ga&lt;sub&gt;0.3&lt;/sub&gt;As</td>
<td>InAs-like Low</td>
</tr>
<tr>
<td>C</td>
<td>GaAs&lt;sub&gt;0.35&lt;/sub&gt;Sb&lt;sub&gt;0.65&lt;/sub&gt;</td>
<td>In&lt;sub&gt;0.7&lt;/sub&gt;Ga&lt;sub&gt;0.3&lt;/sub&gt;As</td>
<td>GaAs-like High</td>
</tr>
</tbody>
</table>
where \( E_{\text{GaAsSb}} \) and \( E_{\text{InGaAs}} \) are CL binding energies of Sb\( 3d_{5/2} \) and In\( 3d_{5/2} \), \( E_{\text{VBM}} \) is the valence band maxima (VBM) of the corresponding samples. \( E_{\text{VBM}} \) was determined by linearly fitting the leading edge of the VB spectra to the base line [63]. \( E_{\text{GaAsSb}}^{\text{InGaAsSb}} - E_{\text{GaAsSb}}^\text{InGaAsSb} \) and \( E_{\text{InGaAs}}^{\text{GaAsSb}} - E_{\text{InGaAs}}^\text{GaAsSb} \) were measured from 150 nm InGaAs/310 nm GaAsSb and 310 nm GaAsSb without the top InGaAs layer, respectively.

\[
\Delta E_{\text{CL}} (i) = E_{\text{GaAsSb}}^{\text{InGaAs}} (i) - E_{\text{InGaAs}}^{\text{GaAsSb}} (i)
\]

is the CL binding energy difference of Sb\( 3d_{5/2} \) and In\( 3d_{5/2} \) measured at the heterointerface from 5 nm InGaAs/310 nm GaAsSb sample of each structure. The conduction band offset (CBO) can be estimated by [63]:

\[
\Delta E_C = E_{\text{GaAsSb}}^g + \Delta E_V - E_{\text{InGaAs}}^g
\]

where \( E_{\text{GaAsSb}}^g \) and \( E_{\text{InGaAs}}^g \) are the band gaps of GaAsSb and InGaAs, respectively. The effective tunneling barrier of the TFET is described as:

\[
E_{\text{beff}} = E_{\text{InGaAs}}^g - \Delta E_V
\]

where \( \Delta E_V \) is the above measured valence band offset.

Based on the measured XPS CL and VBM values and using the Kraut [62] method, the measured VBO (\( \Delta E_V \)), calculated conduction band offset (\( \Delta E_C \)), and \( E_{\text{beff}} \) are summarized in Table 4. Here, \( E_{\text{beff}} \) determines the type of band alignment in the GaAs\( y \)Sb\( 1-y \)/In\( x \)Ga\( 1-x \)As heterostructure, that is, the band alignment is staggered line-up if \( E_{\text{beff}} > 0 \) but broken line-up if \( E_{\text{beff}} < 0 \). Positive effective tunneling barrier height of 0.30 eV and 0.21 eV were determined on structures A (In=0.65, Sb=0.6) and B (In=0.7, Sb=0.65), respectively, indicating a staggered band alignment.

Table 4 Summary of core level to valence band maxima binding energy difference (eV) for GaAsSb and InGaAs, and the binding energy difference between Sb\( 3d_{5/2} \) and In\( 3d_{5/2} \) at the heterointerface (\( \Delta E_{\text{CL}} (i) \)) from the three structures.

<table>
<thead>
<tr>
<th>Structure</th>
<th>( E_{\text{GaAsSb}}^{\text{InGaAsSb}} - E_{\text{GaAsSb}}^\text{InGaAsSb} ) (eV)</th>
<th>( E_{\text{InGaAs}}^{\text{GaAsSb}} - E_{\text{InGaAs}}^\text{GaAsSb} ) (eV)</th>
<th>( \Delta E_{\text{CL}} (i) ) (eV)</th>
<th>( \Delta E_C ) (eV)</th>
<th>( \Delta E_V ) (eV)</th>
<th>( E_{\text{beff}} ) (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>527.66</td>
<td>443.71</td>
<td>83.60</td>
<td>0.35</td>
<td>0.42</td>
<td>0.30</td>
</tr>
<tr>
<td>B</td>
<td>527.70</td>
<td>443.79</td>
<td>83.52</td>
<td>0.39</td>
<td>0.49</td>
<td>0.21</td>
</tr>
<tr>
<td>C</td>
<td>527.59</td>
<td>443.74</td>
<td>83.22</td>
<td>0.63</td>
<td>0.73</td>
<td>-0.03</td>
</tr>
</tbody>
</table>

*The calculated valence offset (\( \Delta E_V \)), conduction band offset (\( \Delta E_C \)), and effective tunneling barrier (\( E_{\text{beff}} \)) are also listed. From Ref. [13].

Figure 31A and B [13] show the schematic band alignments of structures A and B based on the band gap energy values determined above and the experimental results of VBO measured by XPS. One can see from Figure 31A and B that the measured VBO of the intrinsic In\( 0.7 \)Ga\( 0.3 \)As channel layer with respect to the GaAs\( y \)Sb\( 1-y \) source layer are 0.35 eV and 0.39 eV for In (Sb) compositions of 0.65 (0.60) and 0.70 (0.65), respectively. The higher value of VBO for In compositions of 0.7 compared with 0.6 is expected due to the lower band gap of In\( 0.7 \)Ga\( 0.3 \)As. Wang et al. [64] systematically calculated the valence band offsets between most of the III-V semiconductor alloys by a self-consistent band structure method. Using these calculations, the VBO of intrinsic In\( 0.3 \)Ga\( 0.7 \)As relative to intrinsic GaAs\( 0.4 \)Sb\( 0.6 \) as well as intrinsic In\( 0.7 \)Ga\( 0.3 \)As with respect to intrinsic GaAs\( 0.5 \)Sb\( 0.5 \) was determined to be 0.32 eV and 0.34 eV, respectively. The measured VBO values are in close agreement with the calculated values. The difference in VBO values between experimental and calculation may be due to the doping induced band gap narrowing effect in the GaAs\( y \)Sb\( 1-y \) layer. By comparing the effective tunneling barrier height for structures A and B, it can be seen that by increasing In alloy composition from 65% to 70% in the In\( x \)Ga\( 1-x \)As layer and simultaneously increasing Sb alloy composition from 60% to 65% in the GaAs\( y \)Sb\( 1-y \) layer to keep internally lattice matching with respect to each other, the \( E_{\text{beff}} \) value reduces from 0.30 eV to 0.21 eV. Thus, one can modulate the values of \( E_{\text{beff}} \) at the mixed As/Sb based lattice matched heterojunctions (GaAs\( y \)Sb\( 1-y \)/In\( x \)Ga\( 1-x \)As) by carefully controlling both Sb and In compositions. As a result, the mixed As/ Sb based material system is a preferred choice for TFET application as it provides a wide range of compositionally controlled \( E_{\text{beff}} \).

The value of \( E_{\text{beff}} \) can be drastically reduced at the GaAs\( y \)Sb\( 1-y \)/In\( x \)Ga\( 1-x \)As heterojunction if the defect level is high. Figure 31C shows the schematic band alignment of structure C where large amounts of defects were confined at the interface as well as the In\( 0.7 \)Ga\( 0.3 \)As layer [13]. Note that the alloy compositions of In and Sb were the same as that in structure B, except for the higher defect density at the interface as well as in the In\( 0.7 \)Ga\( 0.3 \)As layer in structure C. One can see from Figure 31C [13] that the value of \( E_{\text{beff}} \) is -0.03 eV, suggesting a broken band line-up. It is interesting to note that band alignment was converted from staggered gap (structures A or B) to broken gap (structure C) due to the presence of large amounts of defects in structure C. Figure 31D [13] summarizes the effective tunneling barrier height and the corresponding band alignment types of these three structures.
Figure 31  Schematic energy band diagram of (A) structure A, (B) structure B, and (C) structure C. A type-II staggered band line-up with positive effective tunneling barrier height of 0.30 eV and 0.21 eV was determined at the heterointerface of structures A and B, respectively, whereas a broken band line-up with negative tunneling barrier height of -0.03 eV was found at the heterointerface of structure C. (D) The histogram summarizes the effective tunneling barrier height and the corresponding band alignment types of these structures. Reprinted from Ref. [13], with permission, from the American Institute of Physics, copyright (2012), AIP Publishing LLC.

Previously in Section 4.5, it has been predicted by simulation that fixed positive charges induced by defects at the GaAs$_{1-y}$Sb$_y$/In$_x$Ga$_{1-x}$As heterointerface would bend the energy band and reduce the value of $E_{\text{beff}}$ [11]. If the fixed charge density is large enough ($>6\times10^{12}$/cm$^2$), it will assist band alignment transition from staggered to broken gap in a mixed As/Sb heterostructure [11]. Thus, the experimental data corroborated with the simulation result and confirmed band alignment conversion from staggered to broken gap line-up in a mixed As/Sb TFET heterostructure. Although greater BTBT probability is expected in a broken gap TFET than staggered gap due to the lower tunneling barrier, OFF-state leakage will drastically increase due to the reduced blocking barrier at OFF-state. As a result, reducing defect density at the GaAs$_{1-y}$Sb$_y$/In$_x$Ga$_{1-x}$As interface is indispensable to achieve a tailor-made tunneling barrier height and influence staggered band alignment, without which steep switching and higher $I_{\text{on}}/I_{\text{off}}$ ratio of a TFET device would not be realized.

4.7 Transfer characteristics

The $E_{\text{beff}}$ of the GaAs$_{1-y}$Sb$_y$/In$_x$Ga$_{1-x}$As heterostructure TFET can be modulated by changing Sb and In compositions in each side of the heterostructure, respectively, and different interface engineering will also change the $E_{\text{beff}}$ due to different dislocation densities. To assess the impact of different effective tunneling barrier height and different band alignments on the transfer characteristics of TFET devices, three sets of TFET devices with self-aligned gates were fabricated and tested. Figure 32 [13] shows the room temperature transfer characteristics ($I_{\text{DS}}$-$V_{\text{GS}}$) of TFET devices fabricated from structures A, B, and C as shown in Table 3 measured at $V_{\text{DS}}=0.05$ V and 0.5 V. By comparing the transfer characteristics of TFETs fabricated from structures A and B, it is observed that $I_{\text{on}}$ increased by $\sim2\times$ with the reduction in $E_{\text{beff}}$ from 0.30 eV to 0.21 eV. This is due to the reduced effective tunneling barrier height that enhances the tunneling transmission coefficient [57], which effectively increased BTBT rate and $I_{\text{on}}$ current.
structures A, B, and C at the heterointerface within devices from structure C with structure B, a significant difference in drain current ratio was observed. Besides, the SS is also improved with reducing band gap energy in the source and channel layer should be taken to preserve the staggered band alignment condition \[65\]. In addition, more than four orders in magnitude deterioration of \(I_{\text{off}}/I_{\text{on}}\) ratio was found in the TFET devices fabricated from structure C compared with structure B. The largely increased \(I_{\text{off}}\) and degraded \(I_{\text{off}}/I_{\text{on}}\) ratio indicates that high defect density present at the source/channel interface that assists the transition of band alignment from staggered to broken gap. Measure must be taken to prevent the formation of large amounts of defects at the critical heterointerface during the growth of mixed As/Sb heterostructure TFETs. Consequently, great efforts should be taken to preserve the staggered band alignment with low \(E_{\text{beff}}\); otherwise, all performance improvement of TFETs brought about by \(E_{\text{beff}}\) modulation will be in vain due to band alignment transition.

### 4.8 High temperature reliability of structural properties and device performance

Owing to the low standby voltage and steep SS, the TFET is suitable for low-power applications with a supply voltage lower than 0.5 V. In practice, there is a growing demand for TFETs to be integrated with other devices (e.g., CMOS, optical devices, detectors, etc.) for complex circuit applications. In this regard, the performance of TFETs may be impacted by other devices which can produce heat during operation in the working environment. This leads to the necessity for the transistors to be operated at a high temperature working environment without degradation of device performance. However, for the mixed As/Sb staggered gap TFET structures, due to large lattice mismatch between active layers (GaAs, Sb/InGaAs) and the substrate, there will be some residual strain existing within the active region \[11\]. The residual strain tends to relax during high temperature operation, which will generate dislocations in these layers. Furthermore, fixed charges...
caused by defects and dislocations at the heterointerface [11] will convert energy band alignment from staggered gap to broken gap [14], which will drastically increase $I_{ON}$, and decrease $I_{OFF}$, and this effect is also observed by Zhu et al. [24] in TFETs. Moreover, the high temperature operation may aggravate the intermixing of Sb and As at the GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As heterointerface that will result in uncontrolled layer composition, which may lead to uncontrolled band alignment and may introduce high dislocation density due to compositional mismatch. Besides, high temperature operation may lead to a decrease in band gap of materials in the active layers as well as an increase in channel resistance [48, 66], both of which will influence the ON-state performance of TFET devices [10]. Furthermore, due to the enhanced SRH G-R and the increased TAT process during high temperature operation [23, 24, 37], $I_{OFF}$ may be significantly increased compared with that at room temperature. Therefore, it is necessary to experimentally investigate the reliability of mixed As/Sb staggered gap TFET materials and devices for high temperature operation. Zhu et al. [24] studied both the structural properties and device performance of a GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As staggered gap TFET in the temperature range of 25°C to 150°C. The schematic layer structure of this TFET structure is shown in Figure 17C. The reliability studies of high temperature operation of mixed As/Sb staggered gap TFET material and devices will contribute to better understanding the operation principles within these devices at high operating temperature and will provide important guidance on the material growth optimization and device fabrication for future TFETs.

4.8.1 Strain relaxation properties at high operation temperature

The relaxation state and residual strain of epilayers at each temperature step were obtained from symmetric (004) and asymmetric (115) reflections of RSMs of structure B as shown in Table 3. Figure 33A and B showed symmetric (004) and asymmetric (115) RSMs of the structure at different temperature steps, respectively. Each layer was labeled to its corresponding RLP based on earlier performed wet chemical etching experiments [11]. It can be seen from Figure 33A and B [24] that four distinct RLP maxima were shown in symmetric (004) and asymmetric (115) RSMs at each temperature step, the same as described in Section 4.3.1. Analysis was performed at each temperature step using the symmetric (004) and asymmetric (115) RSMs. Similar strain relaxation values at each temperature step (~75% for In$_{0.5}$Ga$_{0.5}$As, ~82% for GaAs$_{0.35}$Sb$_{0.65}$, and ~72% for In$_{0.7}$Al$_{0.3}$As) as those at 25°C from each epilayer with respect to InP substrate were extracted. The calculated strain relaxation values are summarized in Table 5. The nearly identical strain relaxation states of each epilayer at different temperature steps indicate that the pseudomorphic nature of GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As layers were well maintained and negligible residual strain was relaxed during the high temperature operation. It also indicates that no extra dislocations caused by strain relaxation should be expected during high temperature operation up to 150°C. The similar strain relaxation state of each epilayer during high temperature operation is supported by comparing the position of each RLP with respect to the fully relaxed line in InP structure.

### Table 5

<table>
<thead>
<tr>
<th>Temperature</th>
<th>In$<em>{0.5}$Ga$</em>{0.5}$As</th>
<th>GaAs$<em>{0.35}$Sb$</em>{0.65}$</th>
<th>In$<em>{0.7}$Al$</em>{0.3}$As</th>
</tr>
</thead>
<tbody>
<tr>
<td>25°C</td>
<td>75</td>
<td>81</td>
<td>72</td>
</tr>
<tr>
<td>50°C</td>
<td>79</td>
<td>83</td>
<td>74</td>
</tr>
<tr>
<td>75°C</td>
<td>78</td>
<td>82</td>
<td>73</td>
</tr>
<tr>
<td>100°C</td>
<td>72</td>
<td>81</td>
<td>70</td>
</tr>
<tr>
<td>125°C</td>
<td>77</td>
<td>84</td>
<td>74</td>
</tr>
<tr>
<td>150°C</td>
<td>71</td>
<td>80</td>
<td>69</td>
</tr>
<tr>
<td>Back to 25°C</td>
<td>74</td>
<td>84</td>
<td>71</td>
</tr>
</tbody>
</table>
(the red dashed line) in (115) RSMs at different temperature steps. As shown in Figure 33B [24], almost the same distance from the center of each RLP to the fully relaxed line was observed at different temperatures, indicating nearly identical strain relaxation states of each layer.

It can also be seen from Figure 33A [24] that the RLPs of epilayers were marginally moving away from the InP substrate with increasing temperature. This may be caused by the lattice constant change at higher measurement temperature. The change of lattice parameter of each epilayer recovered after the sample was cooled down to room temperature, which can be confirmed by the RSMs recorded after the temperature cycle. The intensity of each RLP was decreased at high temperature and it was caused by the small displacements of atoms due to thermal vibrations [67]. In fact, the reduction of intensity was recovered when the sample was cooled down to room temperature after temperature cycle. Furthermore, the identical features of (004) and (115) RSMs before and after the temperature cycle measured at 25°C indicate that the strain relaxation properties of this structure does not affect the high temperature operation up to 150°C.

4.8.2 Surface morphology before and after high temperature operation

The 10 μm x 10 μm AFM micrographs of the TFET structure before and after temperature cycle are shown in Figure 34A and B [24], respectively. From Figure 34A and B [24], the anticipated two-dimensional crosshatch patterns were well developed and fairly uniform, as expected for ideal graded buffer [68, 69], from both surfaces before and after high temperature operation. The well-maintained two-dimensional crosshatch patterns and similar surface morphology after the high temperature cycle suggests that the strain within the GaAs0.35Sb0.65/In0.7Ga0.3As layers were not relaxed during the high temperature operation. Otherwise, dislocations would be formed in these layers and the two-dimensional crosshatch pattern developed by the graded buffer will be sheltered by high-density dislocations and a grainy texture with higher surface roughness will be expected [11]. The surface rms roughness before and after temperature cycle were measured to be 3.17 nm and 2.66 nm, respectively. Despite the experimental error, the surface was smoother after high temperature operation. Similar improvements of crystalline quality by high temperature annealing on metamorphic structures were also reported by other researchers where lattice reformation might have resulted in improvements in structural quality [70–72]. In this case, although the annealing temperature was limited to 150°C, the sample was kept at the specific temperature for a long time (~2 h) during the collection of RSM data at each temperature step. The annealing temperature was not set high to relax the residual strain within the epilayers; however, some defects (i.e., point defects) might have annihilated during the long

![Figure 34](image-url) 10 μm x 10 μm AFM surface morphology of the GaAs0.35Sb0.65/In0.7Ga0.3As TFET structure (A) before temperature cycle with rms roughness of 3.17 nm and (B) after temperature cycle with rms roughness of 2.66 nm. Typical crosshatch patterns were observed in both cases. The well-maintained crosshatch pattern and similar surface morphology after the temperature cycle suggests that no significant structural property change was generated in the structure up to 150°C. Reprinted from Ref. [24], with permission, from IEEE.
annealing duration by the redistribution of atoms and hence improve surface morphology. In fact, the improvement of crystalline quality by reduction of defects was also confirmed by a decrease of $p^+-i-n^+$ leakage current of the fabricated TFET devices, which will be discussed in Section 4.8.4.

### 4.8.3 Atom interdiffusion before and after high temperature operation

There could be a potential concern of the mixed As/Sb staggered gap TFET devices for high temperature operation due to the possible intermixing between As and Sb atoms at the source/channel heterointerface. The intermixing between different atoms will be more promoted at higher temperature due to the enhanced ad-atoms diffusion. Besides, high temperature operation may also cause the diffusion of dopant atoms (C) from the heavily doped GaAs$_{0.35}$Sb$_{0.65}$ source to the intrinsic In$_{0.7}$Ga$_{0.3}$As channel layer. This will reduce the abruptness of the doping profile at the tunnel junction, which will in turn reduce the tunneling probability and lead to decrease in $I_{on}$ of TFET devices [10, 23]. To determine the influence of high temperature operation on the junction and doping profiles of the TFET structure, dynamic secondary ion mass spectrometry (SIMS) measurements were performed to characterize the compositional profiles of As, Sb, Ga, In, Si, and C atoms at the interface before and after temperature cycle. Figure 35A [24] showed Ga, In, As, and Sb depth profiles of the TFET structure before temperature cycle, which displayed an abrupt GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As heterointerface. The transition between GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As was <10 nm, within the sputter-induced broadening of the ion beam, indicating low value of As and Sb intermixing at the heterointerface. Figure 35B [24] showed the C and Si doping profiles in the source and drain regions of the TFET structure. An abrupt junction profile was observed at the interfaces. Reprinted from Ref. [24], with permission, from IEEE.

### 4.8.4 Off-state performances at high operation temperature

Temperature-dependent I-V measurements were carried out on the reverse-biased $p^+-i-n^+$ diode with temperatures ranging from 25°C to 150°C with 25°C as a step. Besides, the measurement was repeated at 25°C on the same device after the temperature cycle to determine the influence of the temperature cycle on the OFF-state performance. Figure 37A [24] shows measured leakage current of the reverse-biased $p^+-i-n^+$ diode at different temperature steps. It can be seen from Figure 37A that at each fixed reverse bias, leakage current increased exponentially with increasing temperature, as expected. The variation tendency of $I_{off}$ with temperature was consistent with the SRH-dominated OFF-state transport mechanism, within which the main contribution to the temperature-dependent factor arises from the intrinsic carrier concentration which is proportional to \( \exp(-E_g/2kT) \), where $E_g$
It is interesting to observe that room temperature leakage current of the reverse-biased $p^+-i-n^+$ diode was reduced by almost $2 \times$ after the temperature cycle. This may be due to removal of some deep level traps during high temperature operation. The G-R centers in the mid-gap of bulk materials and within the depletion region of each junction were reduced by atom reformation in the long duration of temperature cycle [72], which will reduce the contribution of SRH G-R current. The improvement of crystalline quality can also be supported by the reduction of $r_{ms}$ roughness after temperature cycle discussed earlier.

is the band gap energy of active layer materials, $k$ is the Boltzmann constant, and $T$ is temperature. To confirm this proposition, numerical simulations were performed using a SRH G-R model to determine the OFF-state transport of the TFET device. All simulations were performed using Sentaurus [58] with temperature ranging from 25°C to 150°C. As shown in Figure 37A (solid lines) [24], the simulated I-V characteristics of the reverse-biased $p^+-i-n^+$ diode is in agreement with the measured data (scattered line) at all temperatures, suggesting the validation of this model. The SRH-dominated OFF-state transport mechanism was also confirmed by the Arrhenius plot, shown in Figure 37B [24]. Extracted activation energy is 0.33 eV, 0.35 eV, and 0.36 eV at a reverse bias of 1 V, 0.5 V, and 0.1 V, respectively. All these values were approximately $E_g/2$ of In$_{0.7}$Ga$_{0.3}$As (≈0.6 eV at 300 K) and GaAs$_{0.65}$Sb$_{0.35}$ (≈0.72 eV at 300 K), indicating that $I_{OFF}$ components of SRH G-R were from both mid-gap interface traps and mid-gap bulk traps.

It is interesting to observe that room temperature leakage current of the reverse-biased $p^+-i-n^+$ diode was reduced by almost $2 \times$ after the temperature cycle. This may be due to removal of some deep level traps during high temperature operation. The G-R centers in the mid-gap of bulk materials and within the depletion region of each junction were reduced by atom reformation in the long duration of temperature cycle [72], which will reduce the contribution of SRH G-R current. The improvement of crystalline quality can also be supported by the reduction of $r_{ms}$ roughness after temperature cycle discussed earlier.
4.8.5 Transfer characteristics at high operation temperature

To gain insight into the switching properties of the mixed As/Sb staggered gap TFETs at high operating temperature, transfer characteristics of these TFET devices were measured at both $V_{GS}$=0.05 V and 0.5 V from 25°C to 150°C using 25°C as a temperature step. Figure 38A [24] showed the transfer characteristics of the TFET device measured at $V_{DS}$=0.05 V with different temperature. As shown in Figure 38A, at low gate voltages (<-0.3 V), the drain current was almost constant without gate modulation, which set the leakage floor of the device, and increased exponentially with rising temperature. With increasing gate voltages from -0.3 V to 0.4 V, the $I_{DS}$ was less temperature-dependent, which indicated that the BTBT current was becoming the dominant current component. For $V_{GS}$>0.4 V, $I_{DS}$ is weak temperature-dependent and it corresponds to the drive current ($I_{DR}$) of the TFET.

To further study the impact of high operating temperature on $I_{DS}$, the $I_{DS}$-$V_{GS}$ characteristics were replotted in a linear scale with $V_{DS}$ from 1.0 V to 1.5 V, as shown in Figure 38B [24]. As can be seen in Figure 38B, $I_{DS}$ has a weak temperature-dependent characteristic corresponding to the BTBT current at the ON-state condition. The inset in Figure 38B [24] shows the changing trend of $I_{DS}$ with temperature at $V_{DS}$=1.5 V. It is interesting to observe that $I_{DS}$ decreases with rising temperature from 25°C to 100°C, but increases from 100°C to 150°C. The former trend of $I_{DS}$ can be explained by the variation of Fermi distribution with temperature and the latter can be explained by the reduction of band gap energy of active region materials as well as the decrease of effective tunneling barrier height. According to Knoch and Appenzeller [18], the tunnel junction acts as a band-pass filter allowing only carriers with energies around the Fermi level in an energy window $\Delta \Phi$ (as shown in Figure 38B and C) to tunnel from source to channel. With increasing temperature, more electrons will be excited to higher energy states, which leads to the decrease in electrons with energies around Fermi level within $\Delta \Phi$, which further results in the reduction of $I_{DS}$ with increasing temperature. Moreover, the source region of the TFET is highly degenerated due to heavily p-type doping. Thus, the degeneracy reduces the number of electrons available for tunneling which reduces ON-state current and degrades SS [17, 22]. In addition, due to the temperature dependence of the Fermi tail caused by heavily p-type doping, the degradation of ON-state current will be more pronounced at high temperature which leads to additional ON-state current loss. However, at a higher temperature of >100°C, the energy window $\Delta \Phi$ will be enlarged by the decrease of band gap energies of the source/channel materials [66]. Furthermore, according to the Kane model [73], also shown in Eq. (8), the $I_{DS}$ of the TFET is directly related to the BTBT generation rate $G_{BTBT}$, which is exponentially related to $-\left(E_{g}\right)^{2}$. The exponential factor of $E_{g}$ predominantly determines the $G_{BTBT}$ on $E_{g}$ and contributes to the increase of $I_{DS}$ with rising temperature from 100°C to 150°C. The increased $I_{DS}$ due to reduction of $E_{g}$ of active region materials may be dominant over the variation of Fermi distribution from 100°C to 150°C. In addition, $E_{g}$ will also reduce due to the reduction of band gap [23], which may provide an extra increase in $I_{DS}$ at higher operation temperature.

Figure 39A [24] shows the transfer characteristics of the same TFET device measured at $V_{DS}=0.5$ V with
different temperatures. As shown in Figure 39A, \( I_{DS} \) is approximately one order higher than that with \( V_{DS} = 0.05 \) V (as shown in Figure 38A), as expected, at each temperature step, which is due to the enhanced electrical field at the tunneling junction brought by higher drain voltage. Similarly, at \( V_{DS} = 0.5 \) V, the OFF-state leakage floor showed strong temperature dependence and the \( I_{DS} \) displayed weak temperature dependence, which indicates that the SRH G-R mechanism and the BTBT processes, respectively, dominated the OFF-state and ON-state transport of the TFET device. To gain better insight into the impact of temperature on \( I_{DS} \), the \( I_{DS}-V_{GS} \) characteristics of the TFET device were replotted in Figure 39B [24] with \( V_{GS} \) from 1.0 V to 1.5 V in a linear scale. The inset in Figure 39B [24] shows the changing trend of \( I_{DS} \) with temperature at \( V_{GS} = 1.5 \) V. A nearly identical changing trend of \( I_{DS} \) with temperature at \( V_{GS} = 0.5 \) V and \( V_{DS} = 0.05 \) V was obtained, indicating that the temperature has a similar effect on the transport mechanism at 0.05 V and 0.5 V drain voltages. \( I_{DS} \) does not increase exponentially with temperatures from 100°C to 150°C, and is different in the case of \( V_{GS} = 0.05 \) V. This might be due to an enhanced electrical field inside the channel brought about by higher drain voltage. Moreover, the enhanced electrical field leads to a larger voltage drop over the channel due to increased channel resistance at a higher temperature of >100°C. As a result, the exponential increase trend of \( I_{DS} \) dominated by the reduction of \( E_o \) is not as remarkable as that with \( V_{DS} = 0.05 \) V. Furthermore, the \( I_{DS}-V_{GS} \) measurements on the same device at 25°C showed similar performance before and after temperature cycle operation both at \( V_{DS} = 0.05 \) V and 0.5 V. It also suggests that no significant structural property change, such as strain relaxation, interdiffusion, etc., took place during high temperature operation up to 150°C within the TFET structure. The \( I_{OFF} \) of the TFET device was reduced after the temperature cycle due to the removal of some trap states.

Figure 40A and B [24] shows the SS and \( I_{MAX}/I_{MIN} \) ratio (\( I_{MAX} \) is \( I_{DS} \) at \( V_{GS} = 1.5 \) V and \( I_{MIN} \) is \( I_{DS} \) at \( V_{GS} = 0.5 \) V) of the TFET device as a function of temperature for \( V_{DS} = 0.05 \) V and 0.5 V, respectively. The value of SS was not sub-60 mV/dec due to high mid-gap traps and surface charges at the channel/high-\( \kappa \) oxide interface. These interface traps and surface charges can delay the Fermi-level movement of the intrinsic channel controlled by \( V_{GS} \), and they can also result in TAT and subsequent thermal emission [23, 55], all of which will degrade SS. For both \( V_{DS} = 0.05 \) V and 0.5 V, SS was almost constant with temperatures up to 100°C, but increases sharply at temperatures >100°C, and it has a strong positive temperature-dependent coefficient from 100°C to 150°C. The strong temperature dependence of SS is caused by TAT in the subthreshold region, in which the electrons in the valence band of the p+ GaAs / InxGa1-xAs source tunneled into the mid-gap traps, followed by subsequent thermal emission into the conduction band of the InxGa1-xAs channel, which gives rise to strong temperature dependence as well as deterioration of SS. To improve SS, surface chemical passivation is essential to suppress these dominant mid-gap traps and surface charges. In addition, SS was improved after temperature cycle for both \( V_{DS} = 0.05 \) V and 0.05 V and it is due to the removal of some trap states during the long duration of annealing. The \( I_{MAX}/I_{MIN} \) ratio decreases exponentially with increasing temperature for both \( V_{DS} = 0.05 \) V and 0.5 V. This can be explained by the combined effects of exponential dependence of \( I_{DS} \), with
temperature and the weak temperature dependence of $I_{ON}$. The $I_{MAX}/I_{MIN}$ ratio decreases from $-10^3$ at 25°C to $-10^5$ at 150°C. This degradation of device performance was mainly due to the high leakage current at higher temperature (>100°C). Moreover, the $I_{MAX}/I_{MIN}$ ratio recovered to its initial level when the device was cooled down to 25°C after temperature cycle, which indicates that the high temperature operation was not destructive to the TFET structure up to 150°C.

In summary, high temperature reliability studies demonstrated stable structural properties and distinguished device characteristics of mixed As/Sb staggered gap TFETs at higher operating temperature. The temperature-dependent structural and device properties of mixed As/Sb staggered gap TFETs highlight the importance of the reliability on high temperature operation of TFETs for future low-power digital logic applications.

## 5 State-of-the-art results of III-V TFETs

Table 6 summarizes the recently reported experimental III-V TFET devices and state-of-the-art performances of TFETs with different band alignments. Dewey et al. [54] first reported a III-V TFET in an experimental setting with a room temperature minimum SS 60 mV/dec (~58 eV/dec) in an $In_{0.53}Ga_{0.47}As$ homojunction using a thin $In_{0.47}Ga_{0.53}As$ pocket layer at the source/channel interface. However, due to the large tunneling barrier within homojunction TFETs, $I_{ON}$ still remains low. Mookerjee et al. and Mohata et al. [9, 15, 77] studied $In_{0.53}Ga_{0.47}As$ homojunction TFETs with different In compositions. Experimental results showed that by increasing In composition from 0.53 to 0.7, $I_{ON}$ increased by 167%, from 24 μA/μm to 60 μA/μm. The increase in $I_{ON}$ is due to the enhanced tunneling probability caused by the reduction of band gap energy. By using $In_{0.53}Ga_{0.47}As$ p'/i high indium composition pocket layers at the source/channel junction as well as using HfO$_2$ as gate oxide, Han et al. [55] reported an $In_{0.53}Ga_{0.47}As$ homojunction TFET with an $I_{ON}$ of 50 μA/μm and room temperature minimum SS of 86 mV/dec. The SS was predicted to be further reduced by eliminating $D_i$ at the HfO$_2$/InGaAs interface. The application of heterojunctions further improved the performance of TFETs, especially in an $In_{0.53}Ga_{0.47}As$/GaAs$_{0.55}$Sb$_{0.45}$ staggered heterostructure. Mohata et al. [9, 57] reported $In_{0.53}Ga_{0.47}As$/GaAs$_{0.55}$Sb$_{0.45}$ staggered TFETs with different effective tunneling barrier height. The effective tunneling barrier height was reduced by increasing In composition in the $In_{0.53}Ga_{0.47}As$ side and increasing Sb composition in the GaAs$_{0.55}$Sb$_{0.45}$ side while keeping the active region ($In_{0.53}Ga_{0.47}As$/GaAs$_{0.55}$Sb$_{0.45}$) to be internally lattice matched. The $I_{ON}$ of fabricated TFETs increased with reduced $E_{gap}$. Besides, the $I_{ON}$ of mixed As/Sb staggered gap TFETs is much higher than that of the homojunction device with the same channel material, which directly demonstrated advantages of this mixed As/Sb staggered gap structure. The $I_{ON}/I_{OFF}$ ratio was also improved by interface engineering. By using GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.3}Ga_{0.7}As$ as source/channel material, Mohata et al. [57] reported a TFET with high $I_{ON}$ of 135 μA/μm with $I_{ON}/I_{OFF}$ ratio of 27,000. The superior device performance indicates the mixed As/Sb $In_{0.53}Ga_{0.47}As$/GaAs$_{0.55}$Sb$_{0.45}$ staggered gap heterostructure as a promising material system to further boost the performance of TFETs.
However, due to the TAT process involved in the transport of the subthreshold region, the SS of mixed As/Sb staggered gap TFETs is not sub-60 mV/dec. As a result, further treatment should be taken to optimize the device fabrication process and additional studies are necessary to find better high-κ dielectric with low interface states and better gate control. Table 6 also summarizes the latest experimental results of mixed As/Sb broken gap (InAs/GaSb or InAs$_{1-y}$Sb$_y$/GaSb) TFETs. As predicted in Section 3.1, utilizing a broken band alignment can even further improve the ON-state performance of TFET devices due to enhanced $I_{\text{ON}}$ by the removal of the tunneling barrier at the source/channel junction. Guangle et al. [74] reported the highest reported $I_{\text{ON}}$ of 380 μA/μm in a TFET using an InAs/GaSb heterostructure with a broken band alignment. Nevertheless, additional measures should be taken to turn OFF these types of devices due to the normally ON properties of the broken gap alignment [38, 78], where it can be reflected by the reduced $I_{\text{ON}}/I_{\text{OFF}}$ ratio from the fabricated devices compared with the staggered gap TFETs. The transfer characteristics of recently reported experimental III-V TFET devices are summarized in Figure 41. The SS of 60 mV/dec is also denoted in Figure 41.

6 Prospects of mixed As/Sb staggered gap TFETs

The $I_{\text{ON}}$ of a TFET is directly related to the tunneling probability at the source/channel junction, which is governed by the $E_{\text{eff}}$. The $E_{\text{eff}}$ of the GaAs$_{1-y}$Sb$_y$/In$_x$Ga$_{1-x}$As material system can be reduced by increasing In composition in In$_x$Ga$_{1-x}$As and Sb composition in GaAs$_{1-y}$Sb$_y$. As a result, a further increase of $I_{\text{ON}}$ in a mixed As/Sb In$_x$Ga$_{1-x}$As/GaAs$_{1-y}$Sb$_y$ staggered gap TFET is expected by modulating the In and Sb compositions to even higher levels at each side. However, higher In and Sb compositions within In$_x$Ga$_{1-x}$As and GaAs$_{1-y}$Sb$_y$ layers, respectively, will lead to larger lattice mismatch between the active layers (In$_x$Ga$_{1-x}$As and GaAs$_{1-y}$Sb$_y$) and the substrate. As a result, the graded buffer layer should be redesigned to accommodate the increased lattice mismatch. In this case, the possibility of generating threading dislocations in the active region will be higher than the structure with less lattice mismatch, as discussed above. Besides, higher Sb composition in the GaAs$_{1-y}$Sb$_y$ layer indicates larger composition change from the Sb-rich GaAs$_{1-y}$Sb$_y$ layer to the As-rich In$_x$Ga$_{1-x}$As layer during MBE growth, and measures must be taken in order to preserve the internally lattice-matched condition. Improper change of group-V fluxes

<table>
<thead>
<tr>
<th>Reference</th>
<th>Channel</th>
<th>Band alignment</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{\text{ON}}$ (μA/μm)</th>
<th>$V_{\text{DS}}$ (V)</th>
<th>$V_{\text{GS}}$ (V)</th>
<th>$V_{\text{ON}}-V_{\text{OFF}}$ (V)</th>
<th>$I_{\text{ON}}/I_{\text{OFF}}$</th>
<th>SS MIN (mV/dec)</th>
<th>SS EFF (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Guangle et al. IEDM, 2012[74]</td>
<td>GaSb</td>
<td>Broken</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>380</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>7500</td>
<td>200</td>
<td>520</td>
</tr>
<tr>
<td>Guangle et al. IEDM, 2012[74]</td>
<td>GaSb</td>
<td>Broken</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>180</td>
<td>0.5</td>
<td>1.5</td>
<td>1.5</td>
<td>6000</td>
<td>300</td>
<td>1200</td>
</tr>
<tr>
<td>Dewey, DRC, 2012[75]</td>
<td>InAsGa$_{1-x}$Sb$_y$</td>
<td>Broken</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>2.3</td>
<td>110</td>
<td>0.5</td>
<td>1.5</td>
<td>3</td>
<td>275</td>
<td>169</td>
<td>310</td>
</tr>
<tr>
<td>Guangle et al. EDL, 2012[76]</td>
<td>In$<em>{0.85}$Ga$</em>{0.15}$</td>
<td>Broken</td>
<td>Al$_2$O$_3$</td>
<td>1.5</td>
<td>135</td>
<td>0.5</td>
<td>1</td>
<td>1.5</td>
<td>169</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>Guangle et al. IEDM, 2011[9]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$</td>
<td>Broken</td>
<td>Al$_2$O$_3$</td>
<td>1.5</td>
<td>85</td>
<td>0.75</td>
<td>1</td>
<td>1.5</td>
<td>60</td>
<td>1000</td>
<td>6000</td>
</tr>
<tr>
<td>Han et al. EDL, 2010[55]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$</td>
<td>Pocket-homojunction</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>24</td>
<td>0.75</td>
<td>1</td>
<td>1.5</td>
<td>27,000</td>
<td>169</td>
<td>380</td>
</tr>
<tr>
<td>Mookerjea et al. IEDM, 2011[15]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$</td>
<td>Pocket-homojunction</td>
<td>TaSiO$_x$</td>
<td>1.1</td>
<td>3</td>
<td>0.3</td>
<td>0.8</td>
<td>15</td>
<td>100</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>Dewey et al. IEDM, 2011[54]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$</td>
<td>Pocket-homojunction</td>
<td>TaSiO$_x$</td>
<td>1.1</td>
<td>5</td>
<td>0.3</td>
<td>0.8</td>
<td>15</td>
<td>100</td>
<td>300</td>
<td></td>
</tr>
</tbody>
</table>

$SS_{\text{MIN}}$ and $SS_{\text{EFF}}$ denote minimum (point) and effective subthreshold slopes, respectively. $SS_{\text{EFF}} = \left(\frac{V_{\text{ON}}-V_{\text{OFF}}}{\log(I_{\text{ON}}/I_{\text{OFF}})}\right)$ [4].
at the heterointerface without changing the compositions more than 2
interface. For the GaAs$_{y}$Sb$_{1-y}$/In$_{x}$Ga$_{1-x}$As heterojunction, GaAs$_{y}$Sb$_{1-y}$ layers at the source/channel interface due to the staggered gap alignment of the material system. The fluxes.
in order to accommodate the larger change of the group-V the substrate. Furthermore, the switching sequence at the date the larger lattice mismatch between active layers and research of mixed As/Sb staggered gap TFETs, new buffer dislocation density in this region. As a result, in the future controlled layer composition, which in turn will produce high intermixing between As and Sb atoms that leads to uncon-

Summary of the transfer characteristics of experimental III-V TFET devices. An SS of 60 mV/dec is also denoted. Reprinted from Refs. [9, 15, 54, 55, 57, 74 – 77], with permission, from IEEE.

Another stratagem to reduce $E_{\text{beff}}$, without significantly increasing lattice mismatch between the active region and the substrate is to insert high In/Sb composition thin pocket layers at the source/channel heterointerface. As reported in an In$_{0.53}$Ga$_{0.47}$As homojunction TFET [55], more than 2x increase in $I_{\text{ON}}$ was obtained by inserting p(6 nm)/i(6 nm) In$_{0.53}$Ga$_{0.47}$As layers at the source/channel interface. For the GaAs$_{y}$Sb$_{1-y}$/In$_{x}$Ga$_{1-x}$As heterojunction, more improvement of $I_{\text{ON}}$ should be expected by inserting high In composition In$_{x}$Ga$_{1-x}$As or high Sb composition GaAs$_{y}$Sb$_{1-y}$ layers at the source/channel interface due to the staggered gap alignment of the material system. The advantage of this approach is that it can modulate the $E_{\text{beff}}$ at the heterointerface without changing the compositions of the entire active area. Therefore, the lattice-mismatch value and strain properties of the active region will be kept similar to the existing structure [15]. As a result, the same graded buffer scheme as well as source/channel/ drain materials can be used for the demonstration of mixed As/Sb staggered gap TFET structures with different $E_{\text{beff}}$ for further increases in $I_{\text{ON}}$. Besides, the thickness of the inserted high composition layer should be below the critical layer thickness so that no lattice mismatch-induced dislocations are expected at the source/channel heterojunction, which guarantees high crystalline quality of the active region.

Furthermore, most fabricated mixed As/Sb staggered gap TFETs show high value of SS due to high interface traps between the gate oxide and the channel [9, 15, 24, 57]. Improved surface passivation chemistry might suppress these dominant mid-gap traps that will improve SS in future TFET devices. A combination of annealing using forming gas and surface cleaning of native oxide are commonly used as a passivation method during the fabrication process [79]. However, higher annealing temperature and longer duration (usually 350°C for 1 h [79, 80]) will introduce the risk of residual strain relaxation within the active layers as well as intermixing of atoms at the heterointerface. Although studies have already demonstrated that the In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.35}$Sb$_{0.65}$ structure can be kept stable up to 150°C, similar stable structural properties might not be guaranteed for structures with higher In/Sb composition at higher temperature. As a result, new surface passivation techniques should be investigated to effectively reduce the interface trap density without introducing any structural property degradation. In addition, further reliability studies should be undertaken to characterize the material properties of new structures at higher temperature.

One of the final objectives of the study of mixed As/Sb staggered gap TFET structure is heterogeneous integration onto Si substrate. Heteroepitaxy of this structure on large diameter, cheaper, and readily available Si substrate will not only offer a path for low-cost and high-performance mixed As/Sb staggered gap TFET but will also significantly increase their yield per die. However, viability of III-V TFET structures on Si relies on the ability to grow high-quality GaAs buffer layers on Si with careful lattice engineering and substrate treatment. The polar-on-nonpolar epitaxy and the 4% lattice mismatch between GaAs and Si may result in the formation of various defects and dislocations. These dislocations can propagate into the active region, significantly changing the band alignment and therefore impeding the performance of the device. Hudait et al. [81–83]
reported heterogeneous integration of In$_{0.7}$Ga$_{0.3}$As and InSb quantum well FETs (QWFETs) on Si substrate and showed excellent electrical quality, which confirmed high quality of active region materials and proved the feasibility of heterogeneous integration of As and Sb based materials and device structures on Si substrate. As a result, mixed As/Sb staggered gap TFETs on Si substrate with similar performances of that on InP substrate will be expected in future research.

In recent years, great efforts have been devoted to boost performances of the mixed As/Sb staggered gap TFET, such as improving $I_{ON}$ [55] and reducing $I_{OFF}$ [57]. However, most of studies were restricted to n-channel TFETs. A study of a high-performance p-channel TFET within the same material system is equally important, without which the energy efficient complementary logic circuits will not be realized. Owing to the ambipolar characteristics of the TFET as described in Section 2.5, the p-type TFET can be achieved by utilizing the n’ side as source and the p’ side as drain. However, optimizations have to be taken during the design of p-channel TFETs to boost ON-state performance and reduce leakage current. For In$_{Ga_{1-x}}$/As/GaAs$_{y}$/Sb$_{1-y}$ staggered gap p-type TFETs, conduction was achieved by the tunneling of holes from the conduction band of the n’ In$_{Ga_{1-x}}$As source to the valence band of the intrinsic GaAs$_y$/Sb$_{1-y}$ channel. Zhu et al. [12] proposed a p-type mixed As/Sb staggered gap TFET structure using an In$_{Ga_{1-x}}$/As/GaAs$_{y}$/Sb$_{1-y}$ heterojunction. This structure shows excellent structural properties with minimum atom interdiffusion at the heterointerface [12]. XPS studies demonstrated an $E_{hff}$ of 0.13 eV, indicating a promising path to achieve high-performance p-channel TFET devices. In the future, investigation of proper high-k dielectric on GaAs$_{0.35}$/Sb$_{0.65}$ channel material should be performed to facilitate the fabrication of p-type TFET devices and enable complementary TFET devices for ultra-low power application.

7 Conclusion

The TFET has been proposed as one of the most promising steep slope switch candidates to be used under a supply voltage below 0.3 V for ultra-low stand power logic applications. The unique band-to-band tunneling transport mechanism enables the TFET to offer significantly reduced SS and thereby lower operation voltage and power dissipation. Using group III-V materials in a TFET structure significantly improves ON-state current and reduces SS due to low band gap energies as well as smaller carrier tunneling mass. The mixed arsenide/antimonide In$_{Ga_{1-x}}$/As/GaAs$_{y}$/Sb$_{1-y}$ heterostructure allows a wide range of band gap energies and various staggered band alignments depending on the alloy compositions in the source and channel materials. Band alignments at the source/channel heterointerface can be well modulated by carefully controlling the compositions in the In$_{Ga_{1-x}}$/As/GaAs$_{y}$/Sb$_{1-y}$ material system. A detailed review of TFETs using mixed As/Sb based heterostructures show superior structural properties and excellent device performance, both of which indicate that the mixed As/Sb staggered gap structure is a promising path for low-standby power application. Experimental results along with device simulations demonstrate potential performance improvement within these heterostructures and leap forward a path to be further optimized. Such TFETs would provide excellent opportunities to be integrated with Si-MOSFETs as ultra-low power devices in an advanced hybrid circuit platform and also provide chances to replace MOSFETs for beyond CMOS applications.

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Yan Zhu received his BS degree in Physics from Shandong University, Jinan, China, and his MS degree in Microelectronics and Solid State Electronics from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China. He is currently working towards his PhD degree in Electrical Engineering at the Bradley Department of Electrical and Computer Engineering, Virginia Tech. His research interests include design and MBE growth of III-V heterostructure tunnel FET structures, material characterization, and device fabrication. He is a student member of Institute of Electrical and Electronics Engineers (IEEE).

Mantu K. Hudait received his MS degree in Materials Science and Engineering from the Indian Institute of Technology, Kharagpur, and his PhD degree in Materials Science and Engineering from the Indian Institute of Science, Bangalore, India in 1999. His PhD dissertation was on the III-V solar cells on Ge and GaAs using metal-organic vapor phase epitaxy. From 2000 to 2005, he was a Postdoctoral Researcher at The Ohio State University and worked on the mixed-cation and mixed-anion metamorphic graded buffer, carrier transport in mixed-anion system, low-band gap thermophotovoltaics, and heterogeneous integration of III-V solar cells on Si using SiGe buffer. From 2005 to 2009, he was a Senior Engineer in the Advanced Transistor and Nanotechnology Group at Intel Corporation. His breakthrough research in low-power and high-speed III-V quantum-well transistor on Si at Intel Corporation was press released in 2007 and 2009. In 2009, he joined the Bradley Department of Electrical and Computer Engineering at Virginia Tech as an Associate Professor. He has over 125 technical publications and refereed conference proceedings and 38 US patents. His research group at Virginia Tech focuses on heterogeneous integration of compound semiconductor based photonic and electronic materials and devices on Si for ultra-low power logic, communication and low-cost photovoltaics. His research interests include III-V compound semiconductor epitaxy, defect engineering in nanoscale, metamorphic buffer, III-V and Ge quantum-well and tunnel transistors and devices for sustainable energy-related applications. He has received two Divisional Recognition Awards from Intel Corporation. He is a member of the American Vacuum Society and the American Society for Engineering Education. He is also a senior member of Institute of Electrical and Electronics Engineers (IEEE).
Graphical abstract

Review: The basic operational principle, key design consideration, and performance optimization are systemically reviewed, as well as the latest simulation results and the state-of-the-art experimental data relating to low-power tunnel field effect transistors using mixed As and Sb based heterostructures are summarized.

Keywords: mixed As and Sb based heterostructures; staggered gap band alignment; tunnel field effect transistors (TFETs).